Description

The μPD72228/28A controller/driver is a peripheral CMOS device designed to interface most microprocessors with a wide variety of dot-matrix LCDs. It can directly drive any multiplexed LCD organized as 8 rows by 50 columns or 16 rows by 42 columns.

The μPD7228/28A has a standby function to conserve power. It is equipped with an 8-bit serial interface, a 4-bit parallel interface, character generators, a 50 x 16 static RAM with full read/write capability, and an LCD timing controller, all of which reduce microprocessor system software requirements.

The μPD7228/28A operates with a single +5-volt power supply and is available in a space-saving 80-pin plastic QFP package.

Features

- LCD direct drive
- 8-or 16-line multiplexing drive possible with single-chip
  - — 8-line multiplexing: 400 (50 x 8) dots
  - — 16-line multiplexing: 672 (42 x 16) dots
- 8-line or 16-line multiplexing drive with n chip configuration
  - — 8-line multiplexing: n x 400 (n x 50 x 8) dots
  - — 16-line multiplexing: n x 800 (n x 50 x 16) dots
- RAM: 2 x 50 x 8 bits for display data storage
- Programmer designated dot (graphics) display
- 5 x 7 dot-matrix display by on-chip character generator
  - — ASCII (alphanumerics, others): 96 characters
  - — JIS (Japan Industrial Standard), Katakana and others: 64 characters.
- Cursor operating command
- 8-bit serial interface compatible with μPD7500, μCOM-87/87LC
- 4-bit parallel interface compatible with μPD7500, μCOM-84/84C
- Standby function
- CMOS technology
- Single +5-volt power supply
- Extended −40 to +85°C temperature range (μPD7228A)

Ordering Information

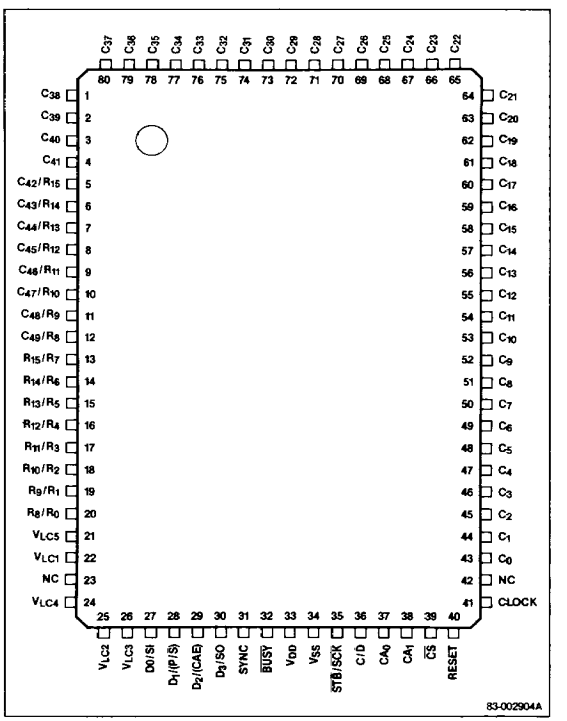
Part No.	Package
μPD7228G-12	80-pin plastic QFP
μPD7228AG-12 (Note 1)	80-pin plastic QFP

Notes:

(1) μPD7228A version has extended temperature range and LCD voltage range.

Pin Configuration

80-Pin Plastic QFP



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Pin Identification

Symbol	Function
C_0-C_{41}	LCD column drive outputs
C_{42}-C_{49}/R_{15}-R_8	LCD column/row drive outputs
R_{15}-R_8/R_7-R_8	LCD row drive outputs
V_{LC1}-V_{LC5}	LCD power supply
NC	No connection
D_0/S_I	Data bus 0/Serial input
D_1(P/$\overline{S}$)	Data bus 1 (Parallel/serial select)
D_2(CAE)	Data bus 2 (Chip address enable)
D_3/SO	Data bus 3/Serial output
SYNC	Synchronization signal input/output
$\overline{BUSY}$	Busy signal output
V_{DD}	Power supply
V_{SS}	Ground
$\overline{STB}/\overline{SCK}$	Strobe/Serial clock input
C/$\overline{D}$	Command/data select input
CA_0, CA_1	Chip address select inputs
$\overline{CS}$	Chip select input
RESET	Reset signal input
CLOCK	System clock input

PIN FUNCTIONS

D_0-D_3 (Data Bus)

In parallel interface mode, D_0-D_3 are input/output pins for 4-bit parallel data. Data on these lines is read at the rising edge of $\overline{STB}$. The 4 bits read on the first $\overline{STB}$ are loaded into the highest 4 bits of the serial/parallel register. The 4 bits read on the second $\overline{STB}$ are loaded into the lowest 4 bits of the register.

The contents of the serial/parallel register are output to these pins on the falling edge of $\overline{STB}$. As in the above case, the high-order 4 bits correspond to the first $\overline{STB}$, and the low-order 4 bits to the second $\overline{STB}$.

In serial interface mode, D_0 is a serial data input pin and D_3 is a serial data output pin. D_1 selects serial or parallel interface mode (P/$\overline{S}$), and D_2 is the chip address enable pin (CAE).

SI Serial Data-In (Input Common to D_0)

In serial interface mode, SI inputs serial data. Data on SI is loaded into the serial/parallel register at the rising edge of $\overline{SCK}$. The first data loaded is the most significant bit. To eliminate noise errors, SI uses the Schmitt-trigger input.

SO Serial Data-Out (Output Common to D_3)

In serial interface mode, SO is an output pin for serial data. The contents of the serial/parallel register are output to the SO pin, beginning with the most significant bit, on the falling edge of $\overline{SCK}$.

P/S Parallel/Serial Select (Input Common to D_1)

This pin sets parallel interface mode if it is high at the falling edge of RESET (at reset release). If it is low at the falling edge of RESET, it selects serial interface mode. The Schmitt-trigger prevents noise errors.

CAE Chip Address Enable (Input Common to D_2)

This pin is used only during serial interface mode; that is, when P/$\overline{S}$ is low at the falling edge of RESET. To enable chip addressing, the CAE line must be high at the falling edge of RESET. In parallel interface mode (when P/$\overline{S}$ is high at the falling edge of RESET), the chip addressing function is enabled regardless of the logic state of CAE at the falling edge of RESET. The Schmitt-trigger input prevents noise errors.

CA_0-CA_1 (Chip Address)

These input pins allow you to address the μPD7228/28A in a multichip configuration used for driving logic displays. During parallel interface mode, CA_0 and CA_1 are compared to chip address data sent from the CPU regardless of CAE status during a reset.

However, during serial interface mode, CA_0 and CA_1 are compared with chip address data from the CPU only when CAE enables chip addressing.

In multichip configurations, the device is selected if $\overline{CS}$ = 0 and CA_0 and CA_1 match the chip address generated by the CPU. This address is the low 2 bits of the first 8-bit data input after $\overline{CS}$ = 0.

In serial interface mode, if chip address selection is not used, connect CA_0 and CA_1 to ground.

$\overline{CS}$ (Chip Select)

$\overline{CS}$ is an active-low chip select input pin. When you are not using the chip address selection function, the $\overline{STB}/\overline{SCK}$ and C/$\overline{D}$ inputs are enabled if a low input is sent to $\overline{CS}$.

When you are using the chip address select function, if $\overline{CS}$ is brought low and the chip address data matches CA_0-CA_1, then $\overline{STB}/\overline{SCK}$ and C/$\overline{D}$ are enabled.

When $\overline{CS}$ is made high, D_0-D_3 and $\overline{BUSY}$ are placed in a high-impedance state. The Schmitt-trigger input prevents noise errors.

$\overline{STB}/\overline{SCK}$ (Strobe/Serial Clock)

In parallel interface mode, this is the strobe signal input pin ($\overline{STB}$) for 4-bit parallel input and output data. In serial interface mode, this is the serial clock input pin ($\overline{SCK}$) for serial input and output data.

C/$\overline{D}$ (Command/Data)

This pin specifies whether the parallel or serial input is a command or data. Bring C/$\overline{D}$ high to input a command, and low to input data.

In parallel interface mode, the contents of C/$\overline{D}$ are latched at the rising edge of the second $\overline{STB}$. Perform any changes to the C/$\overline{D}$ input before the falling edge of the first $\overline{STB}$. When outputting data, hold C/$\overline{D}$ low, whether serial or parallel.

In serial interface mode, the contents of C/$\overline{D}$ are latched at the rising edge of the eighth $\overline{SCK}$.

The Schmitt-trigger input prevents noise errors.

$\overline{BUSY}$ (Busy)

This pin outputs a busy signal to the CPU to warn that the μPD7228/28A is internally busy. When this signal is low, the CPU cannot read/write the μPD7228/28A.

In the parallel interface mode, $\overline{BUSY}$ is forced low at the rising edge of the second $\overline{STB}$. In the serial interface mode, $\overline{BUSY}$ is forced low at the rising edge of the eighth $\overline{SCK}$.

If a chip is deselected ($\overline{CS}$ = high or chip address data does not match), the $\overline{BUSY}$ pin is placed in the high-impedance state.

SYNC (Synchronous)

In a multichip configuration, the SYNC signal synchronizes the phases of the LCD drive ac signals (row/column signal) among all the μPD7228/28A's within the frame period. It uses the row drive signal as a common signal.

If one chip is designated master, its SYNC pin is in output mode and the remaining chips are made slaves. Their SYNC pins are put in input mode. The SMM command selects input or output mode. The master chip outputs a SYNC pulse in the last cycle of each frame. The slave chip reads the SYNC pulse from its own SYNC input for synchronization with the master chip.

In a single-chip configuration, set the SYNC pin in the input or output mode. If you choose input mode, connect the SYNC pin to V_{SS}; conversely, if you choose output mode, the SYNC pin must be open.

Figures 1 and 2 show the output timing for the SYNC pulse in 8- and 16-line multiplexing.

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Figure 1. SYNC Signal in 8-Line Multiplexing

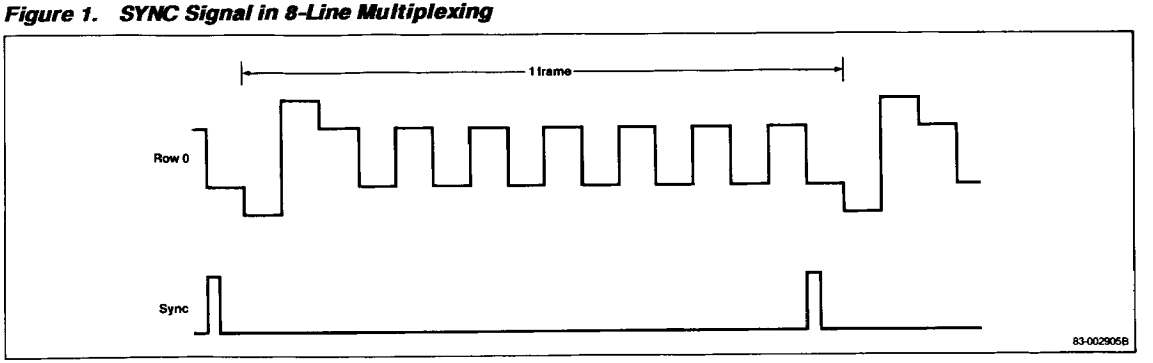
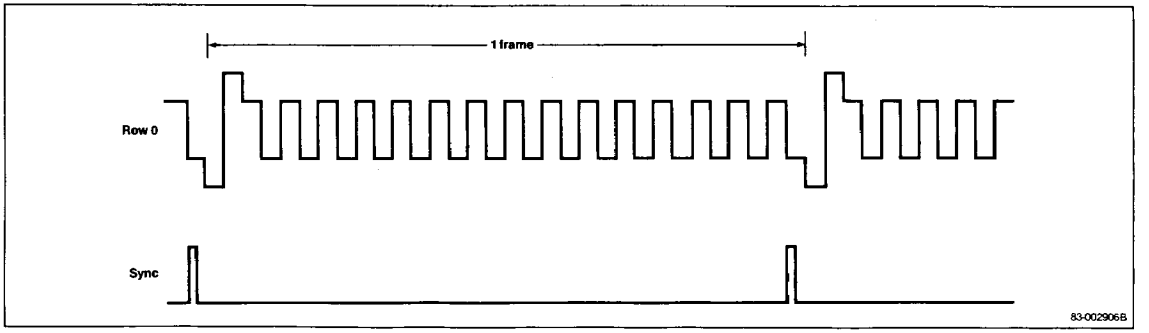


Figure 2. SYNC Signal in 16-Line Multiplexing



C_0-C_{41} (Column)

These pins output the column drive signals for the LCD.

C_{42}-C_{49}/R_{15}-R_8 (Column/Row)

These pins are column drive outputs (C_{42}-C_{49}, 50 x 8 mode) or row drive outputs (R_{15}-R_8, 42 x 16 mode), according to the SMM command.

R_{15}-R_8/R_7-R_0 (Row)

These pins are row drive outputs for rows R_{15}-R_8 or R_7-R_0, according to the SMM command.

V_{LC1}-V_{LC5} (LCD Drive Voltage Supply)

These are reference voltage input pins for determining the voltage level of the LCD column/row drive signals.

CLOCK (Clock)

This is the external clock input pin.

RESET (Reset)

This is the active-high reset signal input pin. It has priority over all operations. You can also use it to release standby mode and begin low power data retention.

V_{DD} (Power Supply)

This is a positive power supply pin.

V_{SS} (Ground)

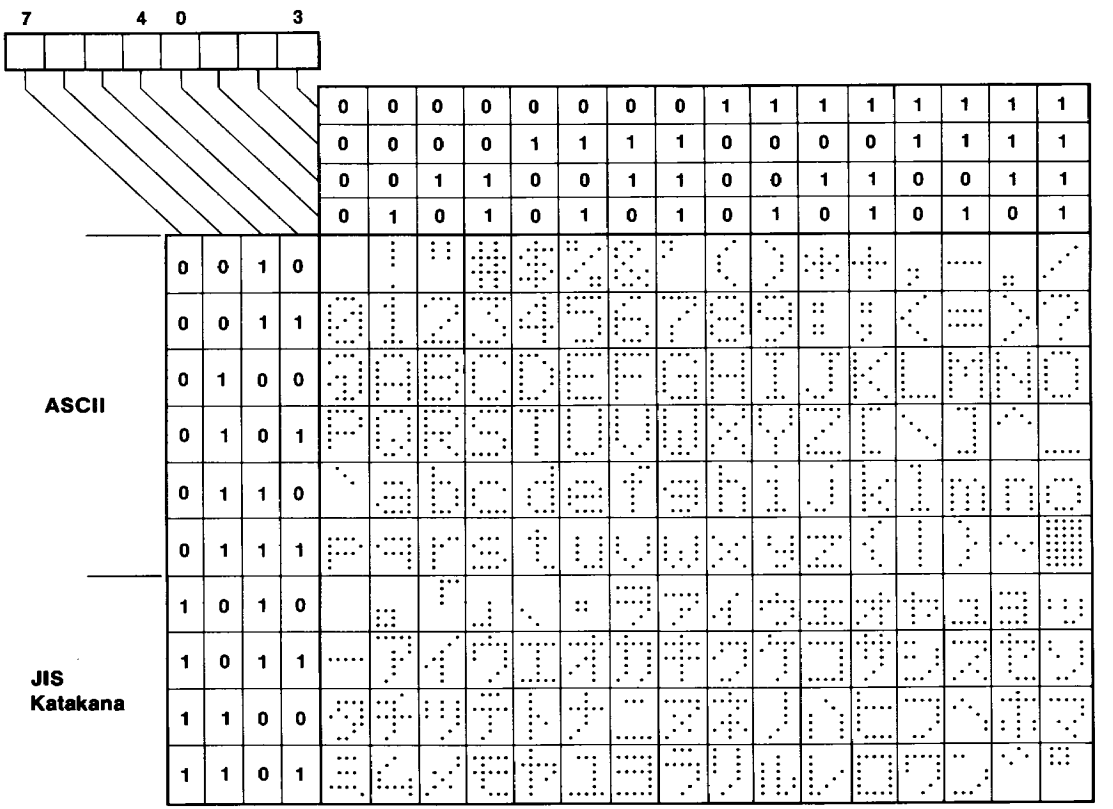
This is ground (GND).

COMMANDS FOR μPD7228/28A

The μPD7228/28A has 16 types of commands, each command consisting of one byte (8 bits).

Figure 3 shows the character codes and display patterns.

Figure 3. Character Codes and Display Patterns



Notes:

(1) The character generator transfers 7-bit dot patterns five times to the five contiguous addresses of data memory.

(2) ASCII Characters, 96 (20H-7FH)

Upper case	26
Lower case	26
Numbers	10
Symbols	34

(3) JIS Characters, 64 (A0H-DFH)

Katakana	55
Symbols	9

(4) Because the character generator does not use bit 7 of data memory, dot R7 in 8 time-division mode and dots R7 and R15 in 16 time-division mode, corresponding to the most significant bits, can be used as cursor independent of the character generator. Use the cursor manipulation commands WRCURS and CLCURS.

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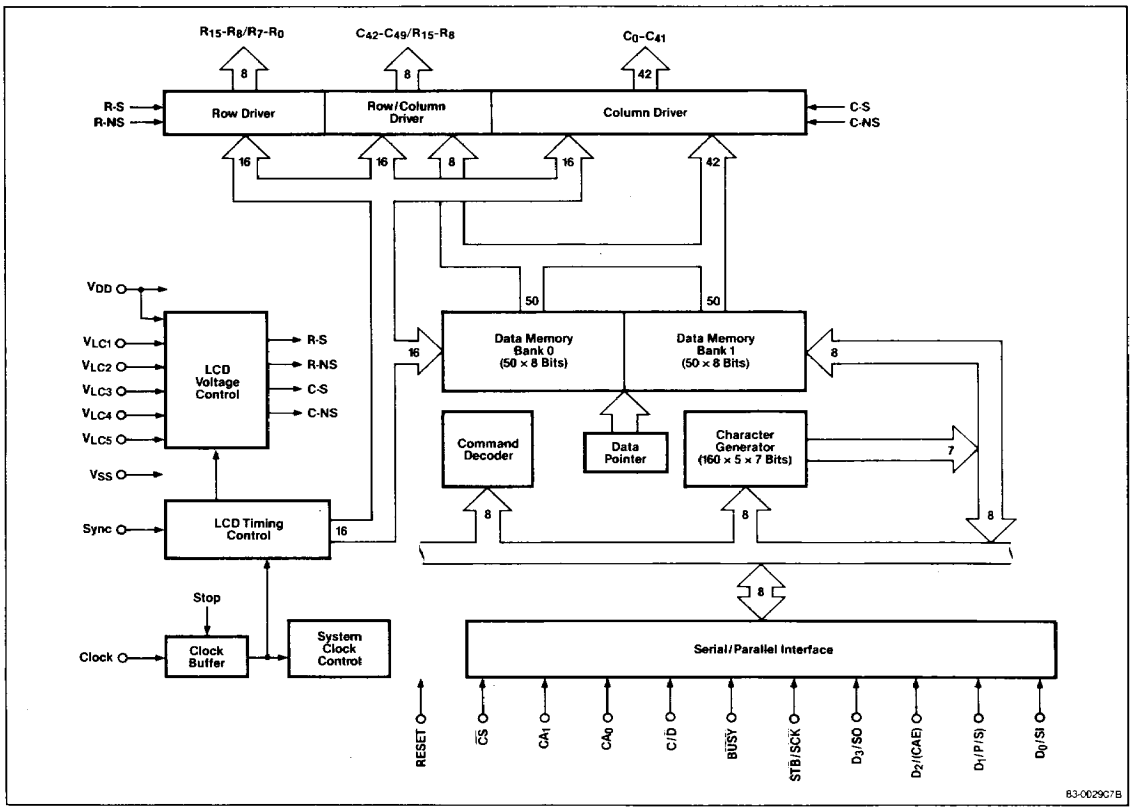
Block Diagram



Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.3 V to +7 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	−0.3 V to V_{DD} +0.3 V
LCD operating voltage, V_{LCD} (7228A)	12.5 V
Operating temperature, T_{OPT}	
7228	−10 to +70°C
7228A	−40 to +85°C
Storage temperature, T_{STG}	−65 to +85°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; V_{DD} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_I			10	pF	Return unmeasured pins to 0 V.
Output capacitance	C_O			25	pF	
I/O capacitance	C_{IO}			15	pF	

DC Characteristics

T_A = −10 to +70°C V_{DD} = +5 V ±10% (μPD7228); T_A = −40 to +85°C; V_{DD} = +5 V ±10% (μPD7228A)

Parameter	Symbol	μPD7228 Min	μPD7228 Typ	μPD7228 Max	μPD7228A Min	μPD7228A Typ	μPD7228A Max	Unit	Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	0.7 V_{DD}		V_{DD}	V	Except $\overline{SCK}$
	V_{IH2}	0.8 V_{DD}		V_{DD}	0.8 V_{DD}		V_{DD}	V	$\overline{SCK}$
Input voltage, low	V_{IL}	0		0.3 V_{DD}	0		0.3 V_{DD}	V	
Output voltage, high	V_{OH1}	V_{DD} − 0.5			V_{DD} − 0.5			V	$\overline{BUSY}$, D_0-D_3; I_{OH} = −400 μA
	V_{OH2}	V_{DD} − 0.5			V_{DD} − 0.5			V	SYNC; I_{OH} = −100 μA
Output voltage, low	V_{OL1}			0.45			0.5	V	$\overline{BUSY}$, D_0-D_3; I_{OL} = 1.7 mA
	V_{OL2}			0.45			0.5	V	SYNC; I_{OL} = 100 μA
Input leakage current, high	I_{LIH}			10			10	μA	V_I = V_{DD}
Input leakage current, low	I_{LIL}			−10			−10	μA	V_I = 0 V
Output leakage current, high	I_{LOH}			10			10	μA	V_O = V_{DD}
Output leakage current, low	I_{LOL}			−10			−10	μA	V_I = 0 V
LCD operating voltage	V_{LCD}	3.0		V_{DD}	V_{DD}		12.5	V	
Row output impedance	R_{ROW}		4	8		6	16	kΩ	
Row/column output impedance	$R_{ROW/COL}$		5	10		7.5	20	kΩ	
Column output impedance	R_{COL}		10	15		15	30	kΩ	
Supply current	I_{DD1}		200	400		250	600	μA	Operating mode; f_C = 400 kHz
	I_{DD2}			20			25	μA	Stop mode; CLK = 0 V

AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10% (μPD7228); T_A = −40 to +85°C; V_{DD} = +5 V ±10% (μPD7228A)

Parameter	Symbol	μPD7228 Min	μPD7228 Typ	μPD7228 Max	μPD7228A Min	μPD7228A Typ	μPD7228A Max	Unit	Conditions
Common Operation									
Clock frequency	f_C	100		1100	100		1100	kHz	
Clock pulse width, high	t_{WHC}	350			350			ns	
Clock pulse width, low	t_{WLC}	350			350			ns	
$\overline{RESET}$ pulse width, high	t_{HRS}	4			4			μs	
$\overline{BUSY}$ delay time from $\overline{CS}$ ↓	t_{DCSB}			2			3	μs	C_L = 50 pF
$\overline{CS}$ ↑ delay time to $\overline{BUSY}$ floating	t_{DCSBF}			4			5	μs	C_L = 50 pF
$\overline{CS}$ high-level time	t_{WHCS}	4			4			μs	
SYNC load capacitance	C_{LSY}			100			100	pF	
Data setup time to RESET ↓	t_{SDR}	0			0			μs	
Data hold time from RESET ↓	t_{HRD}	4			5			μs	
Serial Interface Operation									
$\overline{SCK}$ cycle	t_{CYK}	0.9			0.9			μs	
$\overline{SCK}$ pulse width, high	t_{WHK}	400			400			ns	
$\overline{SCK}$ pulse width, low	t_{WLK}	400			400			ns	
$\overline{SCK}$ hold time from $\overline{BUSY}$ ↑	t_{HBK}	0			0			ns	
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	100			120			ns	

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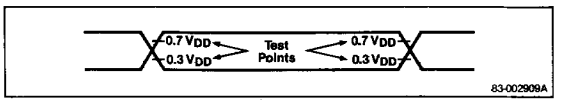
AC Characteristics (cont)

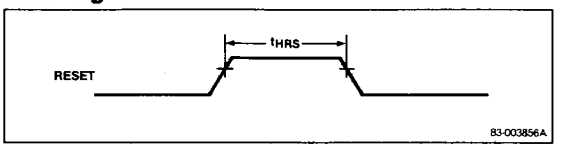
Parameter	Symbol	μPD7228 Min	μPD7228 Typ	μPD7228 Max	μPD7228A Min	μPD7228A Typ	μPD7228A Max	Unit	Conditions
SI hold time from $\overline{SCK}$ ↑	t_{HKI}	250			270			ns	
SO delay time from $\overline{SCK}$ ↓	t_{DKO}			320			350	ns	C_L = 50 pF
$\overline{BUSY}$ delay time from eighth $\overline{SCK}$ ↑	t_{DKB}			3			4	μs	
$\overline{BUSY}$ low-level time	t_{WLB}	18		64	18		64	$1/f_C$	
C/$\overline{D}$ setup time to first $\overline{SCK}$ ↓	t_{SDK}	0			0			μs	
C/$\overline{D}$ hold time from eighth $\overline{SCK}$ ↑	t_{HKD}	2			3			μs	
$\overline{CS}$ hold time from eighth $\overline{SCK}$ ↑	t_{HKCS}	2			5			μs	
Parallel Interface Operation									
Input command setup time to $\overline{STB}$ ↓	t_A	100			120			ns	C_L = 80 pF
Input command hold time from $\overline{STB}$ ↓	t_B	90			110			ns	C_L = 20 pF
Input data setup time to $\overline{STB}$ ↑	t_C	230			250			ns	C_L = 80 pF
Input data hold time from $\overline{STB}$ ↑	t_D	50			70			ns	C_L = 20 pF
Output data delay time	t_{ACC}	90		650	90		750	ns	C_L = 80 pF
Output data hold time	t_H	0		150	0		150	ns	C_L = 20 pF
$\overline{STB}$ pulse width low	t_{SL}	700			700			ns	
$\overline{STB}$ high-level time	t_{SH}	1			1			μs	
$\overline{STB}$ hold time from $\overline{BUSY}$ ↑	t_{HBS}	0			0			μs	
$\overline{BUSY}$ delay time from second $\overline{STB}$ ↑	t_{DSB}			3			4	μs	
C/$\overline{D}$ setup time to first $\overline{STB}$ ↓	t_{SDS}	0			0			μs	
C/$\overline{D}$ hold time from second $\overline{STB}$ ↑	t_{HSD}	2			3			μs	
$\overline{CS}$ hold time from second $\overline{STB}$ ↑	t_{HSCS}	2			3			μs	

Timing Waveforms

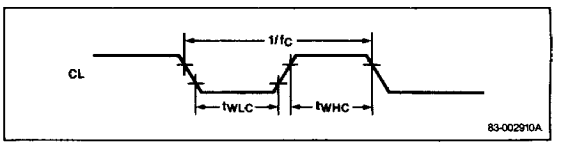
AC Timing Test Points



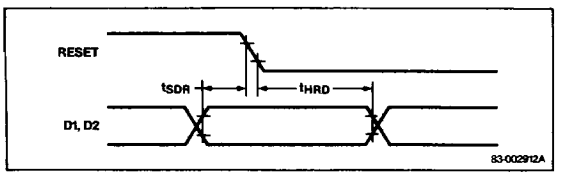
Reset Signal



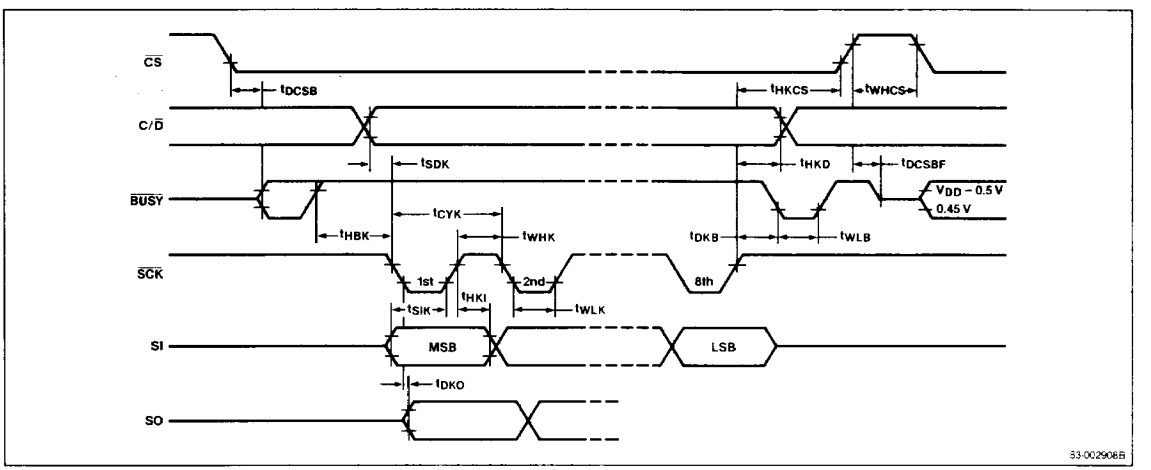
Clock Waveform



Interface



Serial Interface



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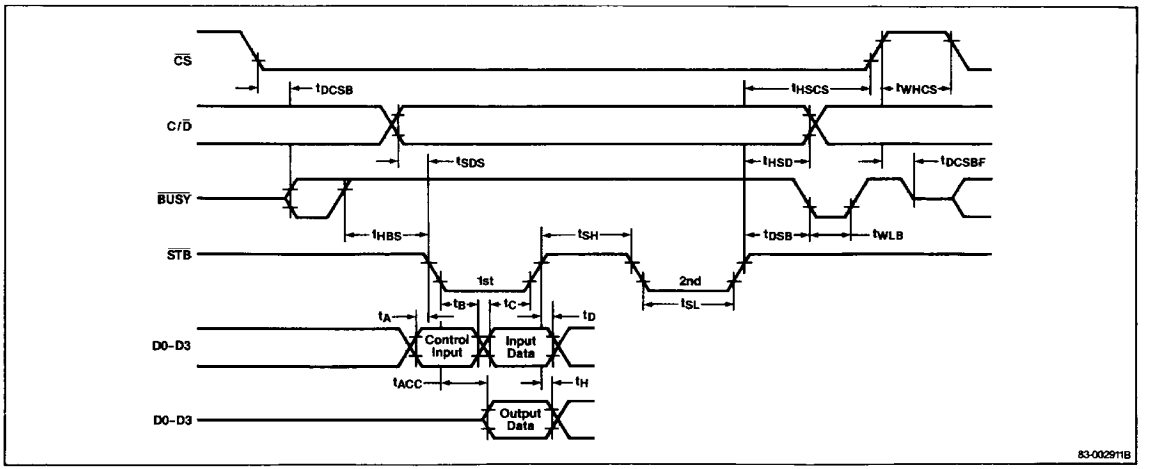
Parallel Interface



Command Summary

Mnemonic	Operation	Instruction Code								Hex Code
SFF	Set frame frequency	0	0	0	1	0	F_2	F_1	F_0	10H-14H
SMM	Set multiplexing mode	0	0	0	1	1	M_2	M_1	M_0	18H-1FH
DISP OFF	Display off	0	0	0	0	1	0	0	0	08H
DISP ON	Display on	0	0	0	0	1	0	0	1	09H
LDPI	Load data pointer with immediate	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0	80H-B1H, C0H-F1H
SRM	Set read mode	0	1	1	0	0	0	I_1	I_0	60H-63H
SWM	Set write mode	0	1	1	0	0	1	I_1	I_0	64H-67H
SORM	Set OR mode	0	1	1	0	1	0	I_1	I_0	68H-6BH
SANDM	Set AND mode	0	1	1	0	1	1	I_1	I_0	6CH-6FH
SCML	Set character mode with left entry	0	1	1	1	0	0	0	1	71H
SCMR	Set character mode with right entry	0	1	1	1	0	0	1	0	72H
BRESET	Bit reset	0	0	1	B_2	B_1	B_0	J_1	J_0	20H-3FH
BSET	Bit set	0	1	0	B_2	B_1	B_0	J_1	J_0	40H-5FH
CLCURS	Clear cursor	0	1	1	1	1	1	0	0	7CH
WRCURS	Write cursor	0	1	1	1	1	1	0	1	7DH
STOP	Set stop mode	0	0	0	0	0	0	0	1	01H

B_2-B_0 Specifies a data memory bit

D_6-D_0 Immediate data

F_2-F_0 Specifies frame frequency as a submultiple of clock frequency

I_1-I_0 Specifies modification of data pointer contents after byte data is processed

J_1-J_0 Specifies modification of data pointer contents after bit is set or reset

M_2-M_0 Specifies data memory bank, number of rows, functions of row/column drivers, and SYNC pin mode