Data Sheet

S6B33B3A

Preliminary

132 RGB Segment & 132 Common Driver For 65,536 Color STN LCD

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Ver. 1.1

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Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.

2. Always test and inspect products under the environment with no penetration of light.

CONTENTS

INTRODUCTION

S6B33B3A is a mid-display-size-compatible driver for liquid crystal dot matrix gray-scale graphic systems. With on-chip RC oscillator circuit, the display-timing signal is generated without being sent from MPU. Also, it is capable of using 8bit/16bit data bus alternatively and operating with 68/80-series MPU in asynchronous. Due to the LCD driving signal (132 RGB X 132 output) corresponding to the display data and the internal bit-map display RAM of 132 ×132 ×16-bit, S6B33B3A is capable of operating max. 132 RGB x 132 dot LCD panels in low-power consumption. Being the segment RGB 3-output, one pixel is 16-bit data and S6B33B3A can max display 65,536 color. SEG charge sharing scheme is applied for low power consumption in module. X-talk compensation scheme is also applied for good display quality.

FEATURES

Driver Output

– 132 RGB x 132

Gray Scale Function

– 65,536 color display of R: 32 gray scale, G: 64 gray scale, B: 32 gray scale
– 4,096 color display of R: 16 gray scale, G: 16 gray scale, B: 16 gray scale

On-chip Display Data RAM

– Capacity: 132 x 16 x 132 = 278.784k bits

Display Mode

– Normal display mode: Entire duty displaying
– Partial display (mode 0, mode 1): Partial duty displaying
– Standby mode: Internal display clocks off
– Area scroll mode: Particular area scrolling

Microprocessor Interface

– 8-bit/16 bit parallel bi-directional interface with 6800-series or 8080-series
– 3/4 Pin SPI (only write operation)

On-chip Low Power Analog Circuit

– On-chip RC oscillator (Internal cap. & external resistor), external clock available
– Voltage converter / Voltage regulator / Voltage follower
– On-chip electronic contrast control (256 steps)

Operating Voltage Range

– VDD : 1.8 ± 0.15 [V] (Typical : 1.8V)
– VDD3: 1.8 to 3.3 [V]
– VIN1: 2.4 to 3.3 [V]
– VIN1R: 2.4 to 3.3[V]
– Display operating voltage(V1): 2.0 to 4.0 [V]

Low Power Consumption

– TBD μA Typ.

Package Type

– COG (Output Pad Pitch Min. 33 μm)

BLOCK DIAGRAM

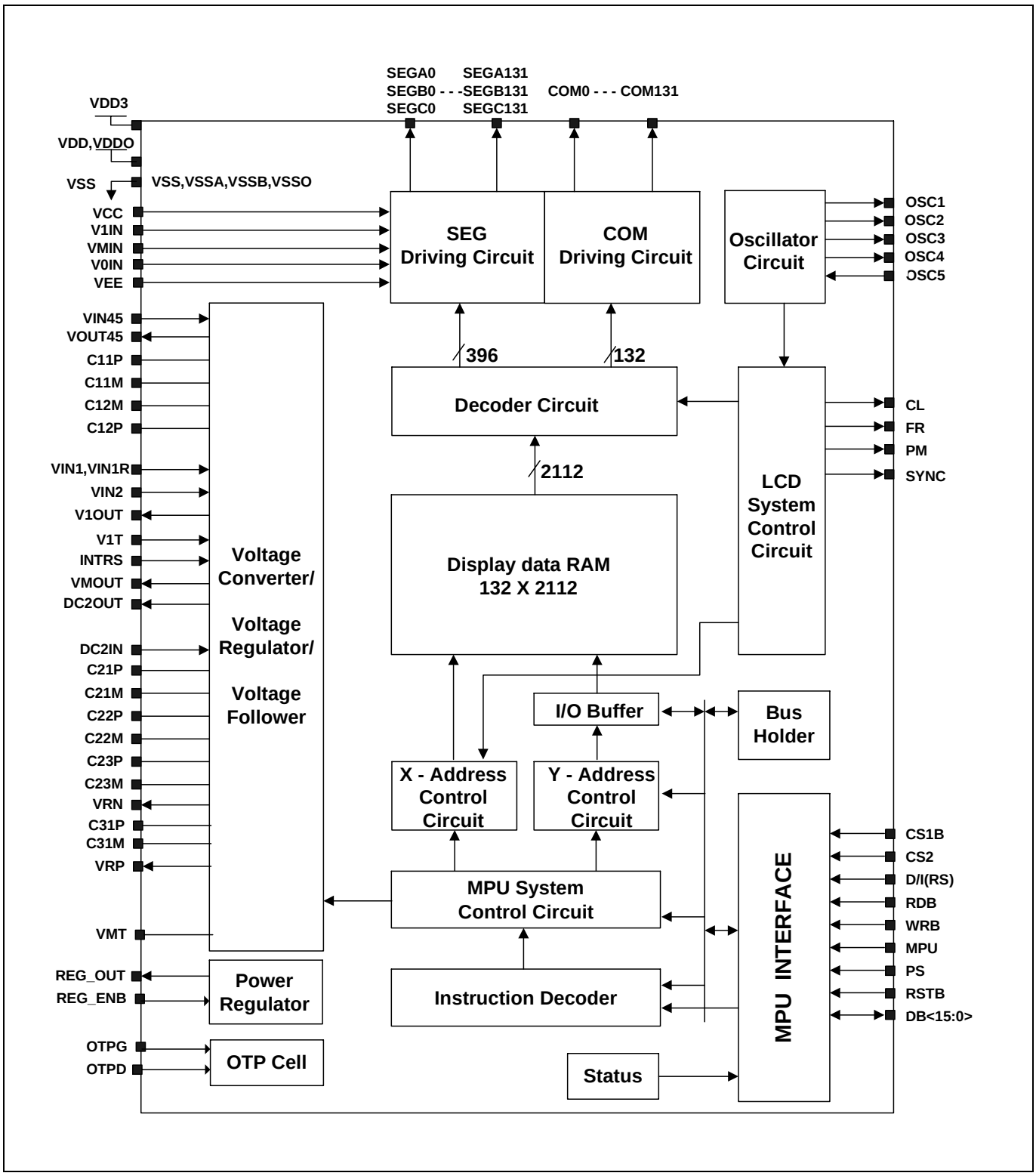


Figure 1. Block Diagram

PAD CONFIGURATION

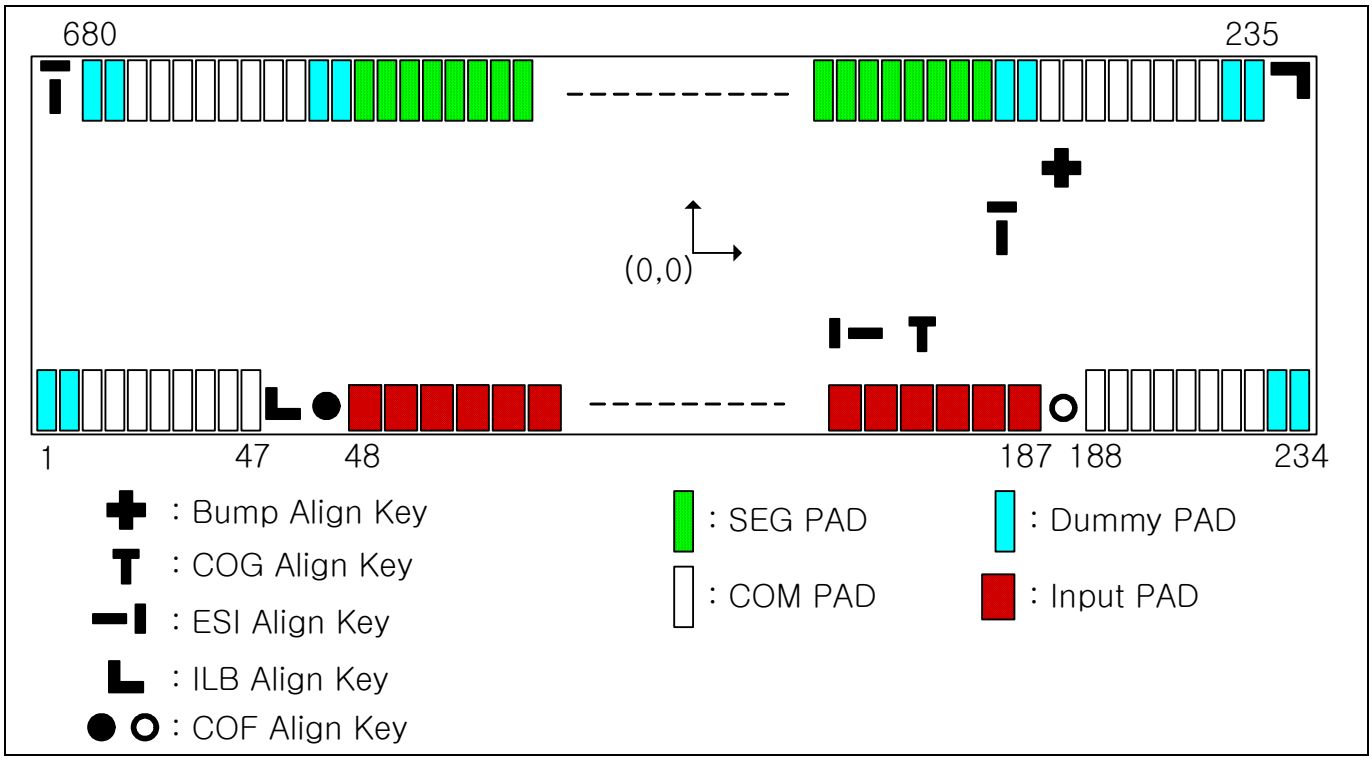


Figure 2. S6B33B3A Chip Pad Configuration

Table 1. S6B33B3A Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size (with S/L 100µm)	-	15150	1700	µm
Pad pitch	100~115	100		
	48~99,116~187	80		
	1~47,188~234,235~680	33		
Bumped pad size	48~187	58	104	
	1~47,188~234,235~680	18	170	
Bumped pad height	All Pad	17		

Figure 3. Bump and COG Align Key Coordinate

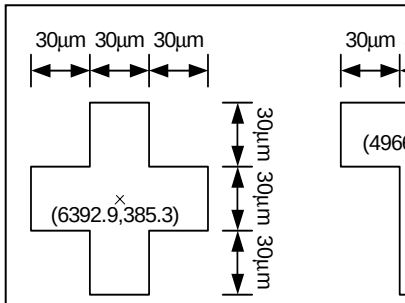


Figure 4. ILB Align Key Coordinate

Figure 5. ESI Align Key Coordinate

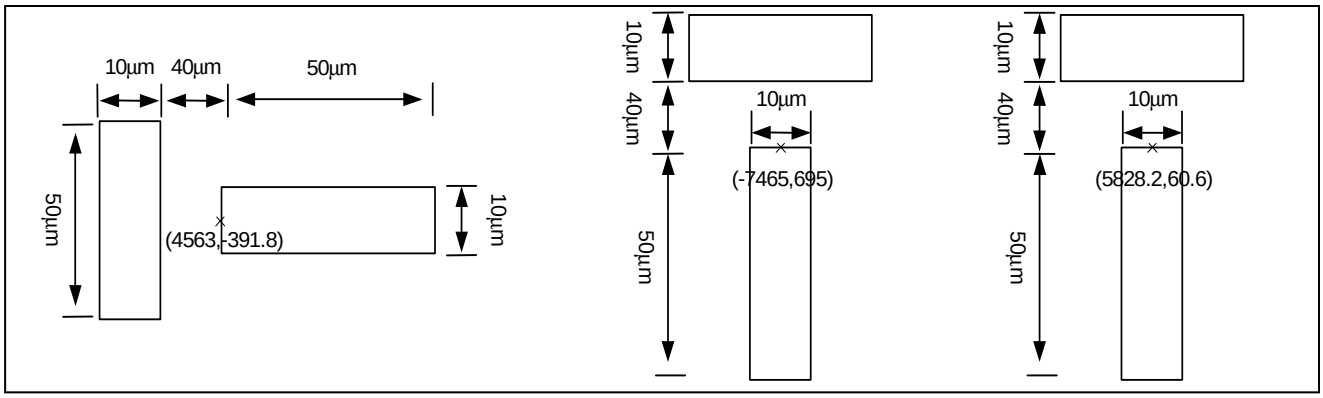
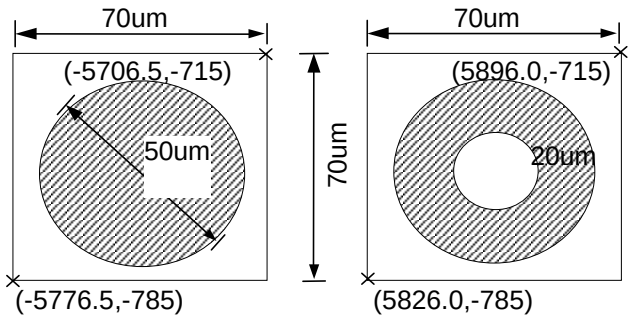


Figure 6. COF Align Key Coordinate



PIN CONFIGURATION

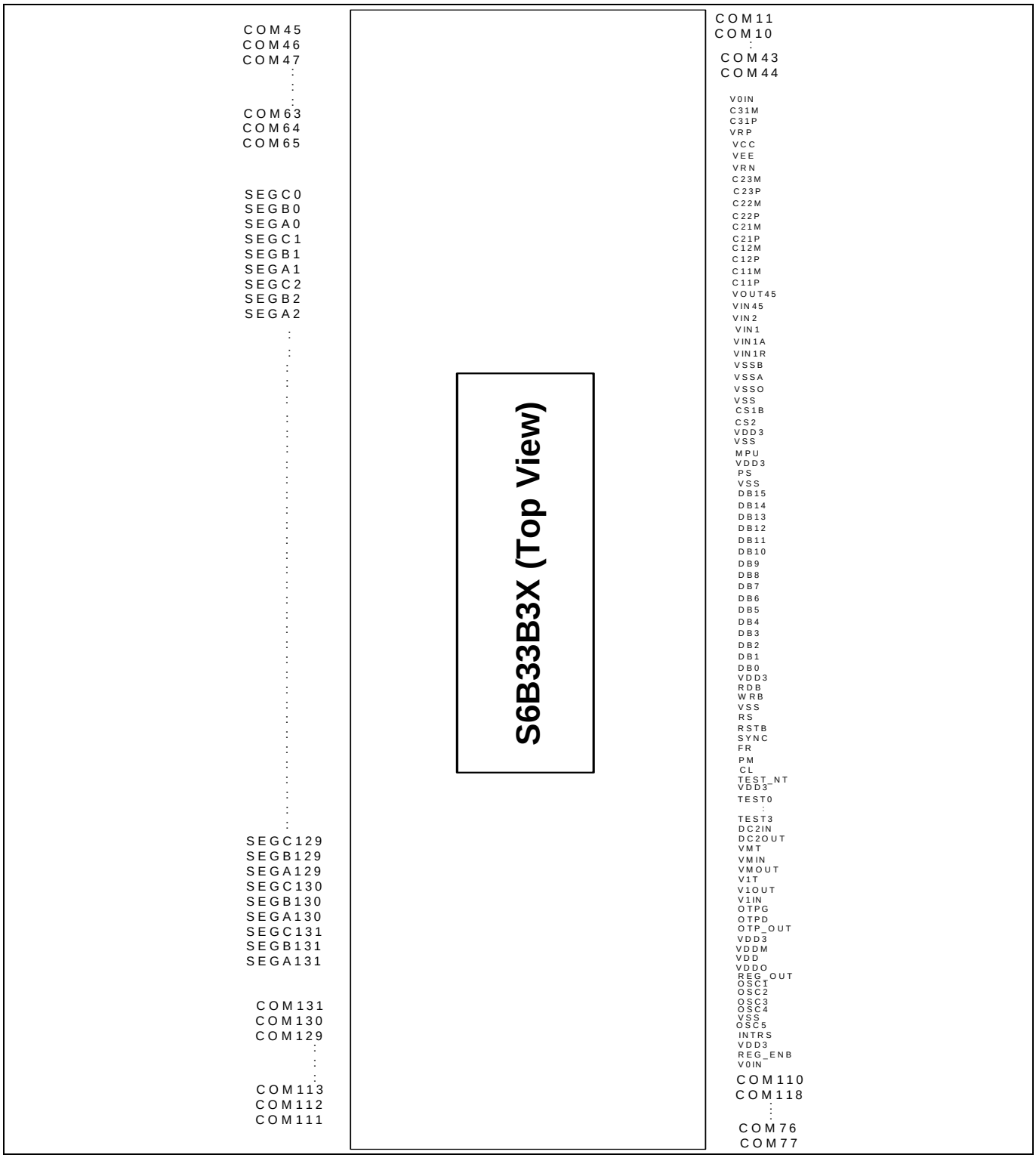


Figure 7. S6B33B3A Chip Pin Configuration

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

NO	X	Y	NAME	NO	X	Y	NAME	NO	X	Y	NAME
1	-7485	-708	DUMMY	51	-5419	-731	INTRS	101	-1399	-731	DB1
2	-7452	-708	DUMMY	52	-5339	-731	OSC5	102	-1299	-731	DB2
3	-7419	-708	COM<77>	53	-5259	-731	VSS	103	-1199	-731	DB3
4	-7386	-708	COM<76>	54	-5179	-731	OSC4	104	-1099	-731	DB4
5	-7353	-708	COM<75>	55	-5099	-731	OSC3	105	-999	-731	DB5
6	-7320	-708	COM<74>	56	-5019	-731	OSC2	106	-899	-731	DB6
7	-7287	-708	COM<73>	57	-4939	-731	OSC1	107	-799	-731	DB7
8	-7254	-708	COM<72>	58	-4859	-731	REG_OUT	108	-699	-731	DB8
9	-7221	-708	COM<71>	59	-4779	-731	REG_OUT	109	-599	-731	DB9
10	-7188	-708	COM<70>	60	-4699	-731	VDDO	110	-499	-731	DB10
11	-7155	-708	COM<69>	61	-4619	-731	VDD	111	-399	-731	DB11
12	-7122	-708	COM<68>	62	-4539	-731	VDD	112	-299	-731	DB12
13	-7089	-708	COM<67>	63	-4459	-731	VDD	113	-199	-731	DB13
14	-7056	-708	COM<66>	64	-4379	-731	VDDM	114	-99	-731	DB14
15	-7023	-708	COM<78>	65	-4299	-731	VDDM	115	1	-731	DB15
16	-6990	-708	COM<79>	66	-4219	-731	VDDM	116	101	-731	VSS
17	-6957	-708	COM<80>	67	-4139	-731	VDD3	117	181	-731	PS
18	-6924	-708	COM<81>	68	-4059	-731	VDD3	118	261	-731	VDD3
19	-6891	-708	COM<82>	69	-3979	-731	VDD3	119	341	-731	MPU
20	-6858	-708	COM<83>	70	-3899	-731	OTP_OUT	120	421	-731	VSS
21	-6825	-708	COM<84>	71	-3819	-731	OTPD	121	501	-731	VDD3
22	-6792	-708	COM<85>	72	-3739	-731	OTPG	122	581	-731	CS2
23	-6759	-708	COM<86>	73	-3659	-731	V1IN	123	661	-731	CS1B
24	-6726	-708	COM<87>	74	-3579	-731	V1IN	124	741	-731	VSS
25	-6693	-708	COM<88>	75	-3499	-731	V1OUT	125	821	-731	VSS
26	-6660	-708	COM<89>	76	-3419	-731	V1T	126	901	-731	VSS
27	-6627	-708	COM<90>	77	-3339	-731	VMOUT	127	981	-731	VSS
28	-6594	-708	COM<91>	78	-3259	-731	VMIN	128	1061	-731	VSS
29	-6561	-708	COM<92>	79	-3179	-731	VMIN	129	1141	-731	VSSO
30	-6528	-708	COM<93>	80	-3099	-731	VMT	130	1221	-731	VSSA
31	-6495	-708	COM<94>	81	-3019	-731	VMT	131	1301	-731	VSSA
32	-6462	-708	COM<95>	82	-2939	-731	DC2OUT	132	1381	-731	VSSA
33	-6429	-708	COM<96>	83	-2859	-731	DC2IN	133	1461	-731	VSSA
34	-6396	-708	COM<97>	84	-2779	-731	TEST3	134	1541	-731	VSSB
35	-6363	-708	COM<98>	85	-2699	-731	TEST2	135	1621	-731	VSSB
36	-6330	-708	COM<99>	86	-2619	-731	TEST1	136	1701	-731	VSSB
37	-6297	-708	COM<100>	87	-2539	-731	TEST0	137	1781	-731	VSSB
38	-6264	-708	COM<101>	88	-2459	-731	VDD3	138	1861	-731	VSSB
39	-6231	-708	COM<102>	89	-2379	-731	TEST_NT	139	1941	-731	VIN1R
40	-6198	-708	COM<103>	90	-2299	-731	CL	140	2021	-731	VIN1A
41	-6165	-708	COM<104>	91	-2219	-731	PM	141	2101	-731	VIN1
42	-6132	-708	COM<105>	92	-2139	-731	FR	142	2181	-731	VIN1
43	-6099	-708	COM<106>	93	-2059	-731	SYNC	143	2261	-731	VIN1
44	-6066	-708	COM<107>	94	-1979	-731	RSTB	144	2341	-731	VIN2
45	-6033	-708	COM<108>	95	-1899	-731	RS	145	2421	-731	VIN2
46	-6000	-708	COM<109>	96	-1819	-731	VSS	146	2501	-731	VIN45
47	-5967	-708	COM<110>	97	-1739	-731	WRB	147	2581	-731	VOUT45
48	-5659	-731	V0IN	98	-1659	-731	RDB	148	2661	-731	C11P
49	-5579	-731	REG_ENB	99	-1579	-731	VDD3	149	2741	-731	C11P
50	-5499	-731	VDD3	100	-1499	-731	DB0	150	2821	-731	C11M

Table 3. Pad Center Coordinates (Continued)

[Unit: μm]

NO	X	Y	NAME	NO	X	Y	NAME	NO	X	Y	NAME
151	2901	-731	C11M	201	6396	-708	COM<31>	251	6812	708	COM<59>
152	2981	-731	C12P	202	6429	-708	COM<30>	252	6779	708	COM<60>
153	3061	-731	C12P	203	6462	-708	COM<29>	253	6746	708	COM<61>
154	3141	-731	C12M	204	6495	-708	COM<28>	254	6713	708	COM<62>
155	3221	-731	C12M	205	6528	-708	COM<27>	255	6680	708	COM<63>
156	3301	-731	C21P	206	6561	-708	COM<26>	256	6647	708	COM<64>
157	3381	-731	C21P	207	6594	-708	COM<25>	257	6614	708	COM<65>
158	3461	-731	C21M	208	6627	-708	COM<24>	258	6581	708	DUMMY
159	3541	-731	C21M	209	6660	-708	COM<23>	259	6548	708	DUMMY
160	3621	-731	C22P	210	6693	-708	COM<22>	260	6515	708	SEGC<0>
161	3701	-731	C22P	211	6726	-708	COM<21>	261	6482	708	SEGB<0>
162	3781	-731	C22M	212	6759	-708	COM<20>	262	6449	708	SEGA<0>
163	3861	-731	C22M	213	6792	-708	COM<19>	263	6416	708	SEGC<1>
164	3941	-731	C23P	214	6825	-708	COM<18>	264	6383	708	SEGB<1>
165	4021	-731	C23P	215	6858	-708	COM<17>	265	6350	708	SEGA<1>
166	4101	-731	DUMMY	216	6891	-708	COM<16>	266	6317	708	SEGC<2>
167	4181	-731	DUMMY	217	6924	-708	COM<15>	267	6284	708	SEGB<2>
168	4261	-731	C23M	218	6957	-708	COM<14>	268	6251	708	SEGA<2>
169	4341	-731	C23M	219	6990	-708	COM<13>	269	6218	708	SEGC<3>
170	4421	-731	VRN	220	7023	-708	COM<12>	270	6185	708	SEGB<3>
171	4501	-731	VRN	221	7056	-708	COM<0>	271	6152	708	SEGA<3>
172	4581	-731	VEE	222	7089	-708	COM<1>	272	6119	708	SEGC<4>
173	4661	-731	VEE	223	7122	-708	COM<2>	273	6086	708	SEGB<4>
174	4741	-731	VEE	224	7155	-708	COM<3>	274	6053	708	SEGA<4>
175	4821	-731	DUMMY	225	7188	-708	COM<4>	275	6020	708	SEGC<5>
176	4901	-731	VCC	226	7221	-708	COM<5>	276	5987	708	SEGB<5>
177	4981	-731	VCC	227	7254	-708	COM<6>	277	5954	708	SEGA<5>
178	5061	-731	VCC	228	7287	-708	COM<7>	278	5921	708	SEGC<6>
179	5141	-731	VRP	229	7320	-708	COM<8>	279	5888	708	SEGB<6>
180	5221	-731	VRP	230	7353	-708	COM<9>	280	5855	708	SEGA<6>
181	5301	-731	C31P	231	7386	-708	COM<10>	281	5822	708	SEGC<7>
182	5381	-731	C31P	232	7419	-708	COM<11>	282	5789	708	SEGB<7>
183	5461	-731	C31M	233	7452	-708	DUMMY	283	5756	708	SEGA<7>
184	5541	-731	C31M	234	7485	-708	DUMMY	284	5723	708	SEGC<8>
185	5621	-731	DUMMY	235	7340	708	DUMMY	285	5690	708	SEGB<8>
186	5701	-731	V0IN	236	7307	708	DUMMY	286	5657	708	SEGA<8>
187	5781	-731	DUMMY	237	7274	708	COM<45>	287	5624	708	SEGC<9>
188	5967	-708	COM<44>	238	7241	708	COM<46>	288	5591	708	SEGB<9>
189	6000	-708	COM<43>	239	7208	708	COM<47>	289	5558	708	SEGA<9>
190	6033	-708	COM<42>	240	7175	708	COM<48>	290	5525	708	SEGC<10>
191	6066	-708	COM<41>	241	7142	708	COM<49>	291	5492	708	SEGB<10>
192	6099	-708	COM<40>	242	7109	708	COM<50>	292	5459	708	SEGA<10>
193	6132	-708	COM<39>	243	7076	708	COM<51>	293	5426	708	SEGC<11>
194	6165	-708	COM<38>	244	7043	708	COM<52>	294	5393	708	SEGB<11>
195	6198	-708	COM<37>	245	7010	708	COM<53>	295	5360	708	SEGA<11>
196	6231	-708	COM<36>	246	6977	708	COM<54>	296	5327	708	SEGC<12>
197	6264	-708	COM<35>	247	6944	708	COM<55>	297	5294	708	SEGB<12>
198	6297	-708	COM<34>	248	6911	708	COM<56>	298	5261	708	SEGA<12>
199	6330	-708	COM<33>	249	6878	708	COM<57>	299	5228	708	SEGC<13>
200	6363	-708	COM<32>	250	6845	708	COM<58>	300	5195	708	SEGB<13>

Table 4. Pad Center Coordinates (Continued)

[Unit: μm]

NO	X	Y	NAME	NO	X	Y	NAME	NO	X	Y	NAME
301	5162	708	SEGA<13>	351	3512	708	SEGB<30>	401	1862	708	SEGC<47>
302	5129	708	SEGC<14>	352	3479	708	SEGA<30>	402	1829	708	SEGB<47>
303	5096	708	SEGB<14>	353	3446	708	SEGC<31>	403	1796	708	SEGA<47>
304	5063	708	SEGA<14>	354	3413	708	SEGB<31>	404	1763	708	SEGC<48>
305	5030	708	SEGC<15>	355	3380	708	SEGA<31>	405	1730	708	SEGB<48>
306	4997	708	SEGB<15>	356	3347	708	SEGC<32>	406	1697	708	SEGA<48>
307	4964	708	SEGA<15>	357	3314	708	SEGB<32>	407	1664	708	SEGC<49>
308	4931	708	SEGC<16>	358	3281	708	SEGA<32>	408	1631	708	SEGB<49>
309	4898	708	SEGB<16>	359	3248	708	SEGC<33>	409	1598	708	SEGA<49>
310	4865	708	SEGA<16>	360	3215	708	SEGB<33>	410	1565	708	SEGC<50>
311	4832	708	SEGC<17>	361	3182	708	SEGA<33>	411	1532	708	SEGB<50>
312	4799	708	SEGB<17>	362	3149	708	SEGC<34>	412	1499	708	SEGA<50>
313	4766	708	SEGA<17>	363	3116	708	SEGB<34>	413	1466	708	SEGC<51>
314	4733	708	SEGC<18>	364	3083	708	SEGA<34>	414	1433	708	SEGB<51>
315	4700	708	SEGB<18>	365	3050	708	SEGC<35>	415	1400	708	SEGA<51>
316	4667	708	SEGA<18>	366	3017	708	SEGB<35>	416	1367	708	SEGC<52>
317	4634	708	SEGC<19>	367	2984	708	SEGA<35>	417	1334	708	SEGB<52>
318	4601	708	SEGB<19>	368	2951	708	SEGC<36>	418	1301	708	SEGA<52>
319	4568	708	SEGA<19>	369	2918	708	SEGB<36>	419	1268	708	SEGC<53>
320	4535	708	SEGC<20>	370	2885	708	SEGA<36>	420	1235	708	SEGB<53>
321	4502	708	SEGB<20>	371	2852	708	SEGC<37>	421	1202	708	SEGA<53>
322	4469	708	SEGA<20>	372	2819	708	SEGB<37>	422	1169	708	SEGC<54>
323	4436	708	SEGC<21>	373	2786	708	SEGA<37>	423	1136	708	SEGB<54>
324	4403	708	SEGB<21>	374	2753	708	SEGC<38>	424	1103	708	SEGA<54>
325	4370	708	SEGA<21>	375	2720	708	SEGB<38>	425	1070	708	SEGC<55>
326	4337	708	SEGC<22>	376	2687	708	SEGA<38>	426	1037	708	SEGB<55>
327	4304	708	SEGB<22>	377	2654	708	SEGC<39>	427	1004	708	SEGA<55>
328	4271	708	SEGA<22>	378	2621	708	SEGB<39>	428	971	708	SEGC<56>
329	4238	708	SEGC<23>	379	2588	708	SEGA<39>	429	938	708	SEGB<56>
330	4205	708	SEGB<23>	380	2555	708	SEGC<40>	430	905	708	SEGA<56>
331	4172	708	SEGA<23>	381	2522	708	SEGB<40>	431	872	708	SEGC<57>
332	4139	708	SEGC<24>	382	2489	708	SEGA<40>	432	839	708	SEGB<57>
333	4106	708	SEGB<24>	383	2456	708	SEGC<41>	433	806	708	SEGA<57>
334	4073	708	SEGA<24>	384	2423	708	SEGB<41>	434	773	708	SEGC<58>
335	4040	708	SEGC<25>	385	2390	708	SEGA<41>	435	740	708	SEGB<58>
336	4007	708	SEGB<25>	386	2357	708	SEGC<42>	436	707	708	SEGA<58>
337	3974	708	SEGA<25>	387	2324	708	SEGB<42>	437	674	708	SEGC<59>
338	3941	708	SEGC<26>	388	2291	708	SEGA<42>	438	641	708	SEGB<59>
339	3908	708	SEGB<26>	389	2258	708	SEGC<43>	439	608	708	SEGA<59>
340	3875	708	SEGA<26>	390	2225	708	SEGB<43>	440	575	708	SEGC<60>
341	3842	708	SEGC<27>	391	2192	708	SEGA<43>	441	542	708	SEGB<60>
342	3809	708	SEGB<27>	392	2159	708	SEGC<44>	442	509	708	SEGA<60>
343	3776	708	SEGA<27>	393	2126	708	SEGB<44>	443	476	708	SEGC<61>
344	3743	708	SEGC<28>	394	2093	708	SEGA<44>	444	443	708	SEGB<61>
345	3710	708	SEGB<28>	395	2060	708	SEGC<45>	445	410	708	SEGA<61>
346	3677	708	SEGA<28>	396	2027	708	SEGB<45>	446	377	708	SEGC<62>
347	3644	708	SEGC<29>	397	1994	708	SEGA<45>	447	344	708	SEGB<62>
348	3611	708	SEGB<29>	398	1961	708	SEGC<46>	448	311	708	SEGA<62>
349	3578	708	SEGA<29>	399	1928	708	SEGB<46>	449	278	708	SEGC<63>
350	3545	708	SEGC<30>	400	1895	708	SEGA<46>	450	245	708	SEGB<63>

Table 5. Pad Center Coordinates (Continued)

[Unit: μm]

NO	X	Y	NAME	NO	X	Y	NAME	NO	X	Y	NAME
451	212	708	SEGA<63>	501	-1438	708	SEGB<80>	551	-3088	708	SEGC<97>
452	179	708	SEGC<64>	502	-1471	708	SEGA<80>	552	-3121	708	SEGB<97>
453	146	708	SEGB<64>	503	-1504	708	SEGC<81>	553	-3154	708	SEGA<97>
454	113	708	SEGA<64>	504	-1537	708	SEGB<81>	554	-3187	708	SEGC<98>
455	80	708	SEGC<65>	505	-1570	708	SEGA<81>	555	-3220	708	SEGB<98>
456	47	708	SEGB<65>	506	-1603	708	SEGC<82>	556	-3253	708	SEGA<98>
457	14	708	SEGA<65>	507	-1636	708	SEGB<82>	557	-3286	708	SEGC<99>
458	-19	708	SEGC<66>	508	-1669	708	SEGA<82>	558	-3319	708	SEGB<99>
459	-52	708	SEGB<66>	509	-1702	708	SEGC<83>	559	-3352	708	SEGA<99>
460	-85	708	SEGA<66>	510	-1735	708	SEGB<83>	560	-3385	708	SEGC<100>
461	-118	708	SEGC<67>	511	-1768	708	SEGA<83>	561	-3418	708	SEGB<100>
462	-151	708	SEGB<67>	512	-1801	708	SEGC<84>	562	-3451	708	SEGA<100>
463	-184	708	SEGA<67>	513	-1834	708	SEGB<84>	563	-3484	708	SEGC<101>
464	-217	708	SEGC<68>	514	-1867	708	SEGA<84>	564	-3517	708	SEGB<101>
465	-250	708	SEGB<68>	515	-1900	708	SEGC<85>	565	-3550	708	SEGA<101>
466	-283	708	SEGA<68>	516	-1933	708	SEGB<85>	566	-3583	708	SEGC<102>
467	-316	708	SEGC<69>	517	-1966	708	SEGA<85>	567	-3616	708	SEGB<102>
468	-349	708	SEGB<69>	518	-1999	708	SEGC<86>	568	-3649	708	SEGA<102>
469	-382	708	SEGA<69>	519	-2032	708	SEGB<86>	569	-3682	708	SEGC<103>
470	-415	708	SEGC<70>	520	-2065	708	SEGA<86>	570	-3715	708	SEGB<103>
471	-448	708	SEGB<70>	521	-2098	708	SEGC<87>	571	-3748	708	SEGA<103>
472	-481	708	SEGA<70>	522	-2131	708	SEGB<87>	572	-3781	708	SEGC<104>
473	-514	708	SEGC<71>	523	-2164	708	SEGA<87>	573	-3814	708	SEGB<104>
474	-547	708	SEGB<71>	524	-2197	708	SEGC<88>	574	-3847	708	SEGA<104>
475	-580	708	SEGA<71>	525	-2230	708	SEGB<88>	575	-3880	708	SEGC<105>
476	-613	708	SEGC<72>	526	-2263	708	SEGA<88>	576	-3913	708	SEGB<105>
477	-646	708	SEGB<72>	527	-2296	708	SEGC<89>	577	-3946	708	SEGA<105>
478	-679	708	SEGA<72>	528	-2329	708	SEGB<89>	578	-3979	708	SEGC<106>
479	-712	708	SEGC<73>	529	-2362	708	SEGA<89>	579	-4012	708	SEGB<106>
480	-745	708	SEGB<73>	530	-2395	708	SEGC<90>	580	-4045	708	SEGA<106>
481	-778	708	SEGA<73>	531	-2428	708	SEGB<90>	581	-4078	708	SEGC<107>
482	-811	708	SEGC<74>	532	-2461	708	SEGA<90>	582	-4111	708	SEGB<107>
483	-844	708	SEGB<74>	533	-2494	708	SEGC<91>	583	-4144	708	SEGA<107>
484	-877	708	SEGA<74>	534	-2527	708	SEGB<91>	584	-4177	708	SEGC<108>
485	-910	708	SEGC<75>	535	-2560	708	SEGA<91>	585	-4210	708	SEGB<108>
486	-943	708	SEGB<75>	536	-2593	708	SEGC<92>	586	-4243	708	SEGA<108>
487	-976	708	SEGA<75>	537	-2626	708	SEGB<92>	587	-4276	708	SEGC<109>
488	-1009	708	SEGC<76>	538	-2659	708	SEGA<92>	588	-4309	708	SEGB<109>
489	-1042	708	SEGB<76>	539	-2692	708	SEGC<93>	589	-4342	708	SEGA<109>
490	-1075	708	SEGA<76>	540	-2725	708	SEGB<93>	590	-4375	708	SEGC<110>
491	-1108	708	SEGC<77>	541	-2758	708	SEGA<93>	591	-4408	708	SEGB<110>
492	-1141	708	SEGB<77>	542	-2791	708	SEGC<94>	592	-4441	708	SEGA<110>
493	-1174	708	SEGA<77>	543	-2824	708	SEGB<94>	593	-4474	708	SEGC<111>
494	-1207	708	SEGC<78>	544	-2857	708	SEGA<94>	594	-4507	708	SEGB<111>
495	-1240	708	SEGB<78>	545	-2890	708	SEGC<95>	595	-4540	708	SEGA<111>
496	-1273	708	SEGA<78>	546	-2923	708	SEGB<95>	596	-4573	708	SEGC<112>
497	-1306	708	SEGC<79>	547	-2956	708	SEGA<95>	597	-4606	708	SEGB<112>
498	-1339	708	SEGB<79>	548	-2989	708	SEGC<96>	598	-4639	708	SEGA<112>
499	-1372	708	SEGA<79>	549	-3022	708	SEGB<96>	599	-4672	708	SEGC<113>
500	-1405	708	SEGC<80>	550	-3055	708	SEGA<96>	600	-4705	708	SEGB<113>

Table 6. Pad Center Coordinates (Continued)

[Unit: μm]

NO	X	Y	NAME	NO	X	Y	NAME
601	-4738	708	SEGA<113>	651	-6388	708	SEGB<130>
602	-4771	708	SEGC<114>	652	-6421	708	SEGA<130>
603	-4804	708	SEGB<114>	653	-6454	708	SEGC<131>
604	-4837	708	SEGA<114>	654	-6487	708	SEGB<131>
605	-4870	708	SEGC<115>	655	-6520	708	SEGA<131>
606	-4903	708	SEGB<115>	656	-6553	708	DUMMY
607	-4936	708	SEGA<115>	657	-6586	708	DUMMY
608	-4969	708	SEGC<116>	658	-6619	708	COM<131>
609	-5002	708	SEGB<116>	659	-6652	708	COM<130>
610	-5035	708	SEGA<116>	660	-6685	708	COM<129>
611	-5068	708	SEGC<117>	661	-6718	708	COM<128>
612	-5101	708	SEGB<117>	662	-6751	708	COM<127>
613	-5134	708	SEGA<117>	663	-6784	708	COM<126>
614	-5167	708	SEGC<118>	664	-6817	708	COM<125>
615	-5200	708	SEGB<118>	665	-6850	708	COM<124>
616	-5233	708	SEGA<118>	666	-6883	708	COM<123>
617	-5266	708	SEGC<119>	667	-6916	708	COM<122>
618	-5299	708	SEGB<119>	668	-6949	708	COM<121>
619	-5332	708	SEGA<119>	669	-6982	708	COM<120>
620	-5365	708	SEGC<120>	670	-7015	708	COM<119>
621	-5398	708	SEGB<120>	671	-7048	708	COM<118>
622	-5431	708	SEGA<120>	672	-7081	708	COM<117>
623	-5464	708	SEGC<121>	673	-7114	708	COM<116>
624	-5497	708	SEGB<121>	674	-7147	708	COM<115>
625	-5530	708	SEGA<121>	675	-7180	708	COM<114>
626	-5563	708	SEGC<122>	676	-7213	708	COM<113>
627	-5596	708	SEGB<122>	677	-7246	708	COM<112>
628	-5629	708	SEGA<122>	678	-7279	708	COM<111>
629	-5662	708	SEGC<123>	679	-7312	708	DUMMY
630	-5695	708	SEGB<123>	680	-7345	708	DUMMY
631	-5728	708	SEGA<123>				
632	-5761	708	SEGC<124>				
633	-5794	708	SEGB<124>				
634	-5827	708	SEGA<124>				
635	-5860	708	SEGC<125>				
636	-5893	708	SEGB<125>				
637	-5926	708	SEGA<125>				
638	-5959	708	SEGC<126>				
639	-5992	708	SEGB<126>				
640	-6025	708	SEGA<126>				
641	-6058	708	SEGC<127>				
642	-6091	708	SEGB<127>				
643	-6124	708	SEGA<127>				
644	-6157	708	SEGC<128>				
645	-6190	708	SEGB<128>				
646	-6223	708	SEGA<128>				
647	-6256	708	SEGC<129>				
648	-6289	708	SEGB<129>				
649	-6322	708	SEGA<129>				
650	-6355	708	SEGC<130>				

PIN DESCRIPTION

Table 7. Power Supply Pins

Name	I/O	Description
VDD3	Supply	Main power supply
VIN1R	Supply	Internal regulator power supply This pin is connected to VIN1.
VDD	Supply	Regulated power supply input pin for internal digital block. This pin is connected to REG_OUT outside the chip with stabilization capacitor. When the internal regulator is not used, VDD should be tied to external 1.8V directly.
VDDO	Supply	Oscillator power supply, this pin is connected to VDD.
VDDM	Supply	Display Data RAM power supply, this pin is connected to VDD.
VSS VSSO VSSA VSSB	GND	Ground
V1IN	I	LCD segment high selected driving voltage input pin
V1OUT	O	LCD segment high driving voltage output pin
VMIN	I	LCD common non-selected driving voltage input pin
VMOUT	O	LCD common non-selected driving voltage output pin
V0IN	I	LCD segment low selected driving voltage input pin
VCC	I	LCD common high selected driving voltage input pin
VRP	O	LCD common high selected driving voltage output pin
VEE	I	LCD common low selected driving voltage input pin The relationship between VCC, V1, VM, V0 and VEE: VCC > V1 > VM > V0(=VSS) > VEE (V1 - VM = VM – V0, VCC –VM = VM - VEE)
VRN	O	LCD common low selected driving voltage output pin
VIN1 VIN1A	I	Power supply for 1’st booster circuit and VM amp
VIN2	I	Power supply for 2’nd booster circuit
VOUT45	O	1’st booster output pin
VIN45	I	Power supply for V1. Connect to VOUT45 or VIN1
C11P C11M C12P C12M	O	External capacitor connection pins used for 1’st booster circuit
V1T	I	Thermistor resistor connection pin
INTRS	I	External resister select pin for temperature compensation circuit - INTRS = L : External resistor mode, INTRS = H : Internal resistor mode
DC2IN	I	Power supply for 2’nd booster. Connect to DC2OUT pin
DC2OUT	O	Power output pin for 2’nd booster input
C21P C21M C22P C22M C23P C23M	O	External capacitor connection pins used for 2’nd booster circuit
C31P C31M	O	External capacitor connection pins used for 3’rd booster circuit

VMT	I	External capacitor connection pins used for segment charge sharing

Table 8. MPU Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin.
When RSTB is “L”, initialization is executed.</td></tr>
<tr><td rowspan="6">PS
MPU</td><td rowspan="6">I</td><td>PS, MPU interface select pin
<table><tr><th>PS</th><th>MPU</th><th>Description</th></tr><tr><td>H</td><td>L</td><td>8080-series parallel interface</td></tr><tr><td>H</td><td>H</td><td>6800-series parallel interface</td></tr><tr><td>L</td><td>L</td><td>3 pin SPI (Write only)</td></tr><tr><td>L</td><td>H</td><td>4 pin SPI (Write only)</td></tr></table></td></tr>
<tr><td>NOTE : In serial mode, WRB and RDB must be fixed to either VDD3 or VSS.</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. When chip select is non-active, DB0 to DB15 may be high impedance.</td></tr>
<tr><td>D/I
(RS)</td><td>I</td><td>Data / Instruction select input pin
– D/I = “H”: DB0 to DB15 are display data
– D/I = “L”: DB0 to DB7 are instruction data</td></tr>
<tr><td rowspan="3">WRB
(R/W)</td><td rowspan="3">I</td><td>Read / Write execution control pin
<table><tr><th>PS</th><th>MPU</th><th>MPU Type</th><th>WRB</th><th>Description</th></tr><tr><td>H</td><td>H</td><td>6800-series</td><td>R/W</td><td>Read / Write control input pin
– R/W = “H”: read
– R/W = “L”: write</td></tr><tr><td>H</td><td>L</td><td>8080-series</td><td>WRB</td><td>Write enable clock input pin
The data on DB0 to DB15 are latched at the rising edge of the WRB signal.</td></tr></table></td></tr>
<tr><td></td></tr>
<tr><td></td></tr>
<tr><td rowspan="3">RDB
(E)</td><td rowspan="3">I</td><td>Read / Write execution control pin
<table><tr><th>PS</th><th>MPU</th><th>MPU Type</th><th>RDB</th><th>Description</th></tr><tr><td>H</td><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– R/W = “H”: When E is “H”, DB0 to DB15 are in an output status.
– R/W = “L”: The data on DB0 to DB15 are latched at the falling edge of the E signal.</td></tr><tr><td>H</td><td>L</td><td>8080-series</td><td>RDB</td><td>Read enable clock input pin
When RDB is “L”, DB0 to DB15 are in an output status.</td></tr></table></td></tr>
<tr><td></td></tr>
<tr><td></td></tr>
<tr><td>DB[15:8]
DB[7]/SDI
DB[6]/SCL
DB[5:0]</td><td>I/O</td><td>-DB[15:0]: 16-bit bi-directional data bus.
-SDI: Serial data input pin. The data is latched at the rising edge of SCL.
-SCL: Serial clock input pin.
When these pins are not used according to mode, these pins must be connected to VDD3 or VSS.</td></tr>
</table>

Table 9. Oscillator and Power Regulator Pins

Name	I/O	Description
OSC1 OSC2	O	CR oscillator output pin When the internal CR oscillator is used, connect to OSC1 through a resistor. OSC1 – OSC2: Using in normal display mode, partial display mode 0 When an external oscillator is used, OSC1 pin is connected to VSS or VDD3
OSC3 OSC4	O	CR oscillator output pin When the internal CR oscillator is used, connect to OSC3 through a resistor. OSC3 – OSC4: Using in partial display mode 1 When an external oscillator is used, OSC3 pin is connected to VSS or VDD3
OSC5	I	External clock input pin When an external input is used, it is input to this pin. But the internal oscillator is used, this pin is connected to VDD3 or VSS.
REG_ENB	I	Internal regulator enable/disable input pin - REG_ENB = “L” (tied to VSS) : enable internal regulator - REG_ENB = “H” (tied to VDD3) : disable internal regulator
REG_OUT	O	Internal voltage regulator output pin The regulator output port from this pin is used as a power supplier for an internal digital block via VDD pins.

Table 10. Timing signal Pins for monitoring

Name	I/O	Description
CL	O	Shift clock output pin
PM	O	Field delimiter output pin
SYNC	O	Frame output pin
FR	O	Liquid crystal alternating current output pin

Table 11. LCD driver output pins

Name	I/O	Description
SEGA0 to 131	O	LCD driving segment output (Red or Blue)
SEGB0 to 131	O	LCD driving segment output (Green)
SEGC0 to131	O	LCD driving segment output (Blue or Red)
COM0 to 131	O	LCD common outputs

Table 12. OTP pins

Name	I/O	Description
OTPG	I	Power of writing OTP cell (When this pin is not used, this pin must be floating)
OTPD	I	Power of writing OTP cell (When this pin is not used, this pin must be floating)
OTP_OUT	O	Don't' use this pin. maker's test pin This pin must be floating.

Table 13. Test pins

Name	I/O	Description
TEST[3:0]	I	Don't use these pins. IC maker's test pins These pins must be tied to VDD3, not VDD.
TEST_NT	O	Don't use this pin. IC maker's test pin This pin must be floating.

FUNCTIONAL DESCRIPTION

MPU INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B33B3A can interface with an MPU only when CS1B is “L” and CS2 is “H”. When these pins are set to any other combination, D/I, RDB, and WRB inputs are disabled and DB0 to DB15 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel/Serial Interface

The S6B33B3A has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table14.

Table 14. Parallel/Serial Interface-Mode

PS	MPU	CS1B	CS2	MPU bus type
H	L	CS1B	CS2	8080-Series MPU
	H			6800-Series MPU
L	L	CS1B	CS2	3–Pin SPI
	H			4-Pin SPI

Parallel Interface (PS=”H”)

The 8-bit/16-bit bi-directional data bus is used in parallel interface. The type of MPU is selected by MPU and the mode of data-bus is controlled by 16B register as shown in below. In accessing internal registers (D/I = “L”), only DB[7:0] are valid. When 16B is low, DB[15:8] are high impedance.

Table 15. Microprocessor Selection for Parallel Interface

MPU	16B	CS1B	CS2	RDB	WRB	Data Bus	MPU bus type
L	L	CS1B	CS2	RDB	WRB	DB[15:0]	8080-series MPU
	H					DB[7:0]	
H	L	CS1B	CS2	E	R/W	DB[15:0]	6800-series MPU
	H					DB[7:0]	

Table 16. Parallel Data Transfer

D/I	6800-series		8080-series		Description
	E	R/W	RDB	WRB	
H	H	H	L	H	Read display data
H	H	L	H	L	Write display data
L	H	H	L	H	Read out internal status register
L	H	L	H	L	Write instruction data

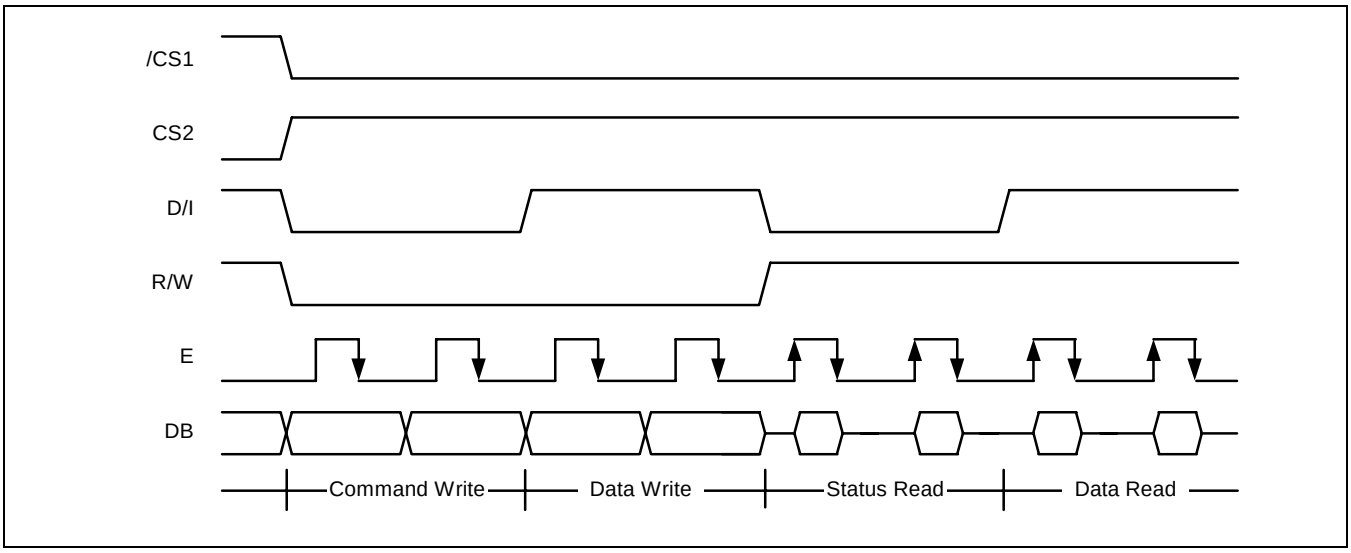


Figure 8. 6800-Series MPU Interface protocol (MPU="H")

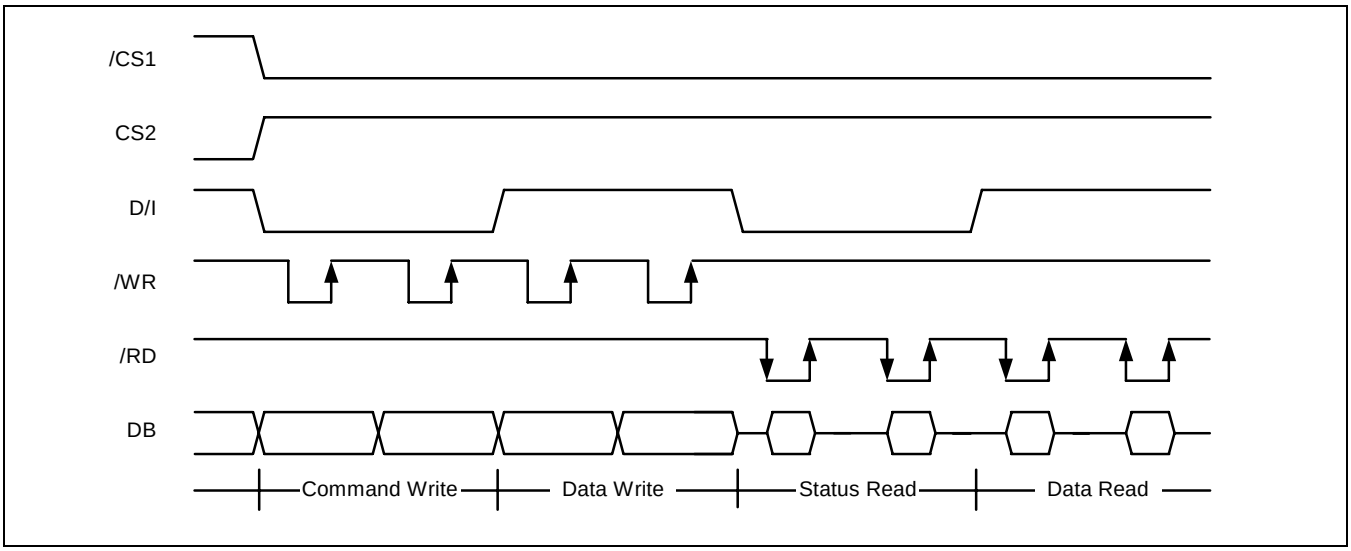


Figure 9. 8080-Series MPU Interface Protocol (MPU="L")

Serial Interface (PS=”L”)

Communication with the microprocessor occurs via a clock-synchronized serial peripheral interface when PS is low. When using the serial interface, read operations are not allowed. When the chip select inputs are valid (CS1B = “L” & CS2 = “H”), the serial data is sent most significant bit first on the rising edge of a serial clock going into DB6 and processed as 8 bit parallel data on the eighth clock. Since the clock signal is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended. And Invalid, the internal shift register and the counter are reset.
The serial interface type is selected by setting PS as shown in Table17.

Table 17. Microprocessor Selection for Serial Interface

PS	MPU	CS1B	CS2	D/I	Serial Data	Serial Clock	SPI Mode
L	L	CS1B	CS2	By S/W	DB[7]	DB[6]	3-Pin
	H	CS1B	CS2	D/I			4-Pin

3-Pin SPI Interface (PS = "L" & MPU = "L")

In 3-Pin SPI Interface mode, the first bit of serial 9bits is used to indicate whether serial data input is display or instruction data instead of D/I pin. The serial data format consists of D/I (1bit) and DATA (8bits). For details, refer the Figure 10.

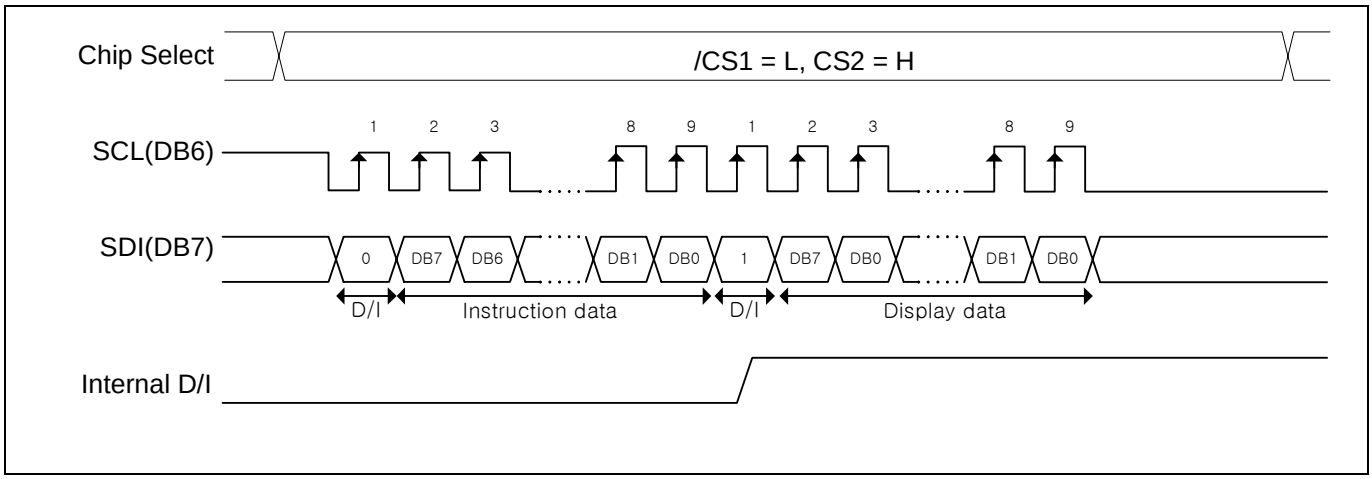


Figure 10. 3-Pin SPI Timing (D/I is not used)

4-Pin Serial Interface (PS="L" & MPU="H")

In 4-pin SPI interface mode, D/I pin is used for indicating whether serial data input is display or instruction data. Data is display data when D/I is high and instruction data when D/I is low. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. For details, refer the Figure 11.

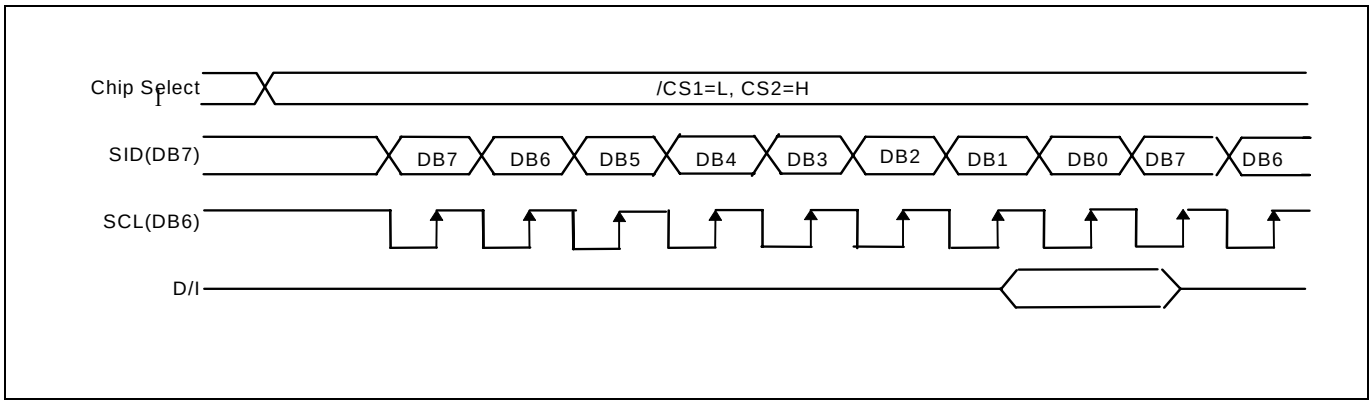


Figure 11. 4-Pin Serial Interface Timing

DISPLAY DATA RAM

The on-chip display data RAM of S6B33B3A is a static RAM that is stored the data for the display. It is a 2,112 x 132 structure. It is controlled by 2 addresses, X and Y. And, RAM area selection and automatic address count up functions are accomplished by the internal instructions.

DDRAM Address Area Selection

A part of DDRAM address area of S6B33B3A can be accessed by X and Y address area settings. After setting RAM area, the addresses become the start address.

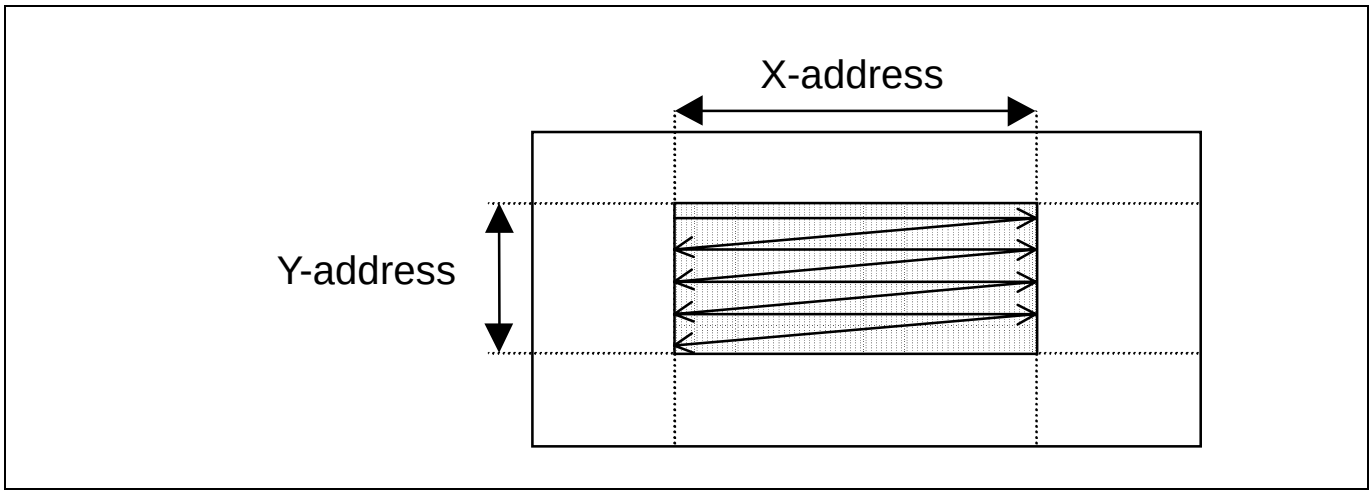


Figure 12. DDRAM Address Area

Table 18. Y address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	0	0	0	1	0
P1	Y start address set(Initial Status = 00H)							
P2	Y end address set(Initial Status = 83H)							

Table 19. X address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	0	0	0	1	1
P1	X start address set (Initial status = 00H)							
P2	X end address set (Initial status = 83H)							

RAM Addressing Count up

By selecting the X address and Y address area by the internal instructions, the address counts up from its start address to end address after data access operation. When one address is equal to the end address, it returns to the start address. At this time, the other address is increased by 1.

X address count mode (X address = 00h to 83h, Y address = 00h to 83h)

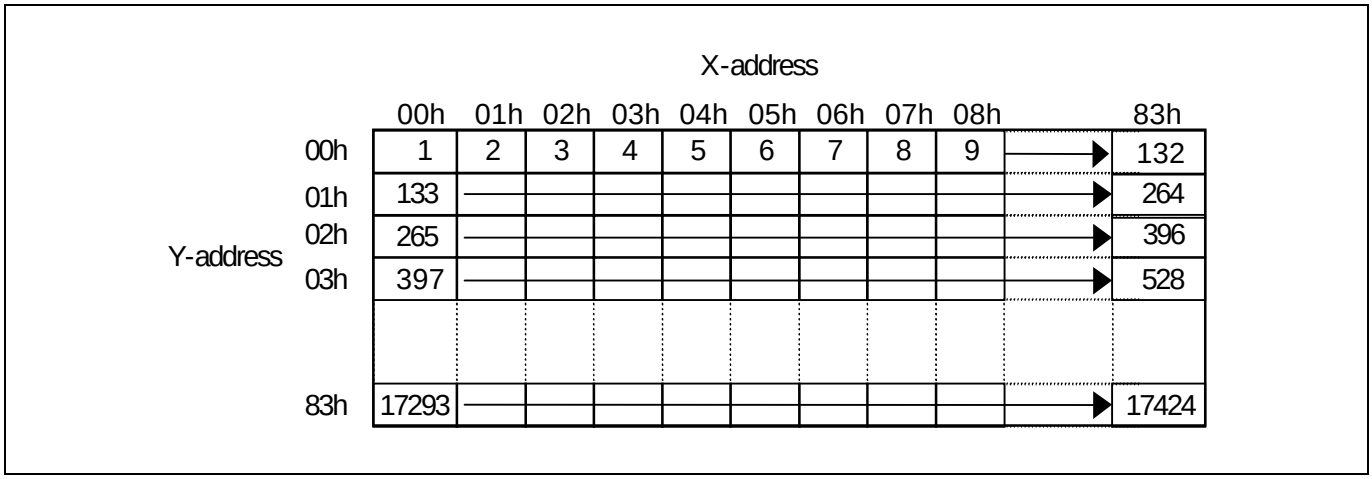


Figure 13. X address count mode

Y address count mode (X address =00h to 83h, Y address = 00h to 83h)

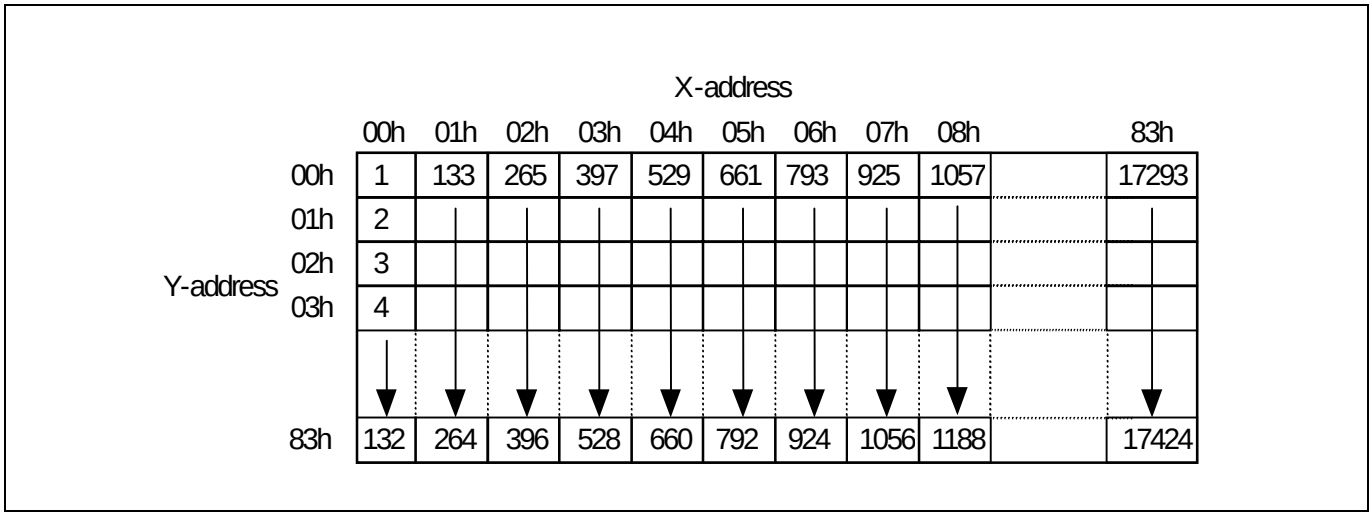


Figure 14. Y address count mode

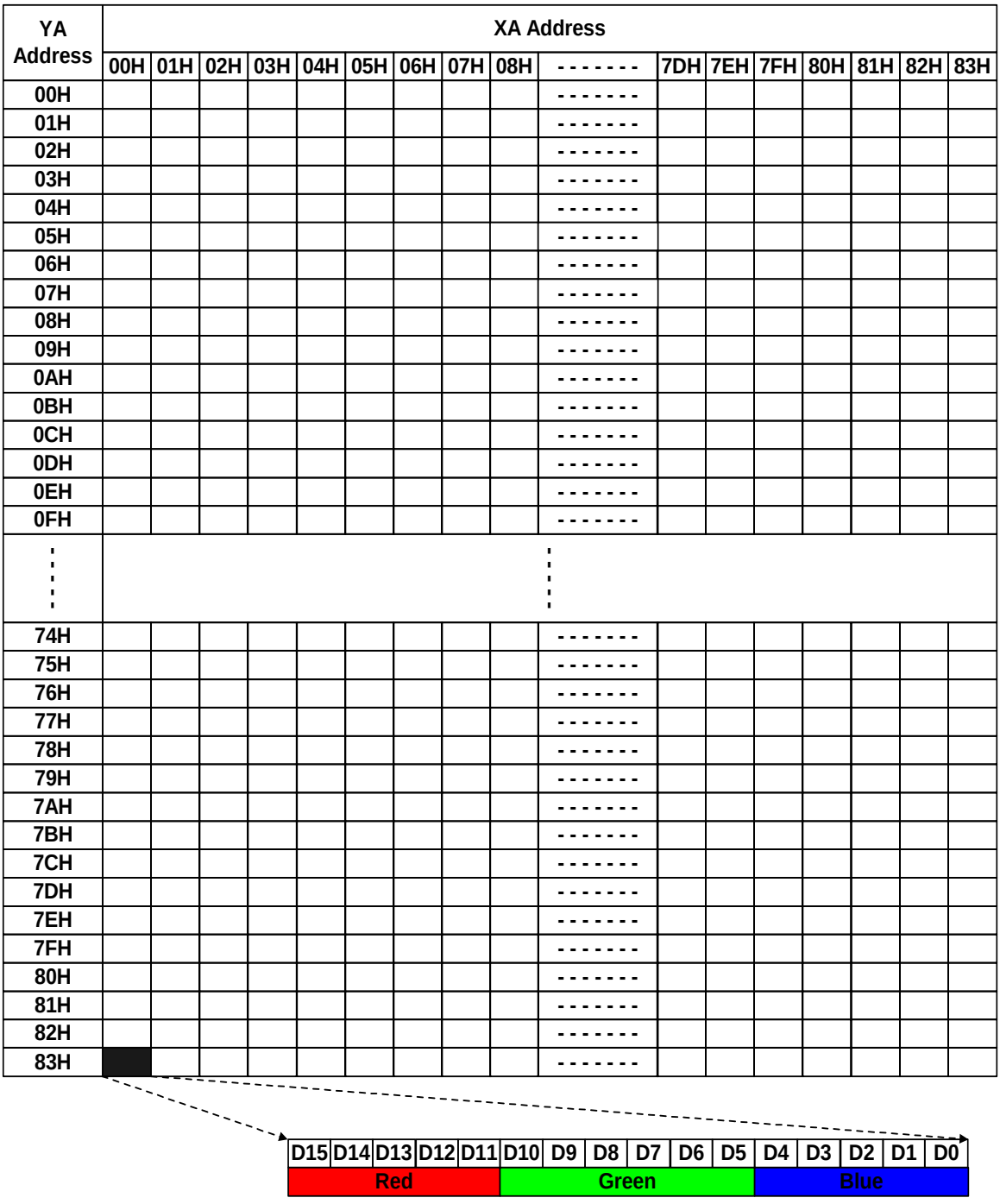


Figure 15. Display Data RAM Map

Partial Display Mode

The S6B33B3A realizes the partial display function with low duty driving for saving power consumption and showing the various display duties. It is set as display start/end line number.

Area Scroll Function

The S6B33B3A realizes the specific area scroll function. (1/132 duty case).

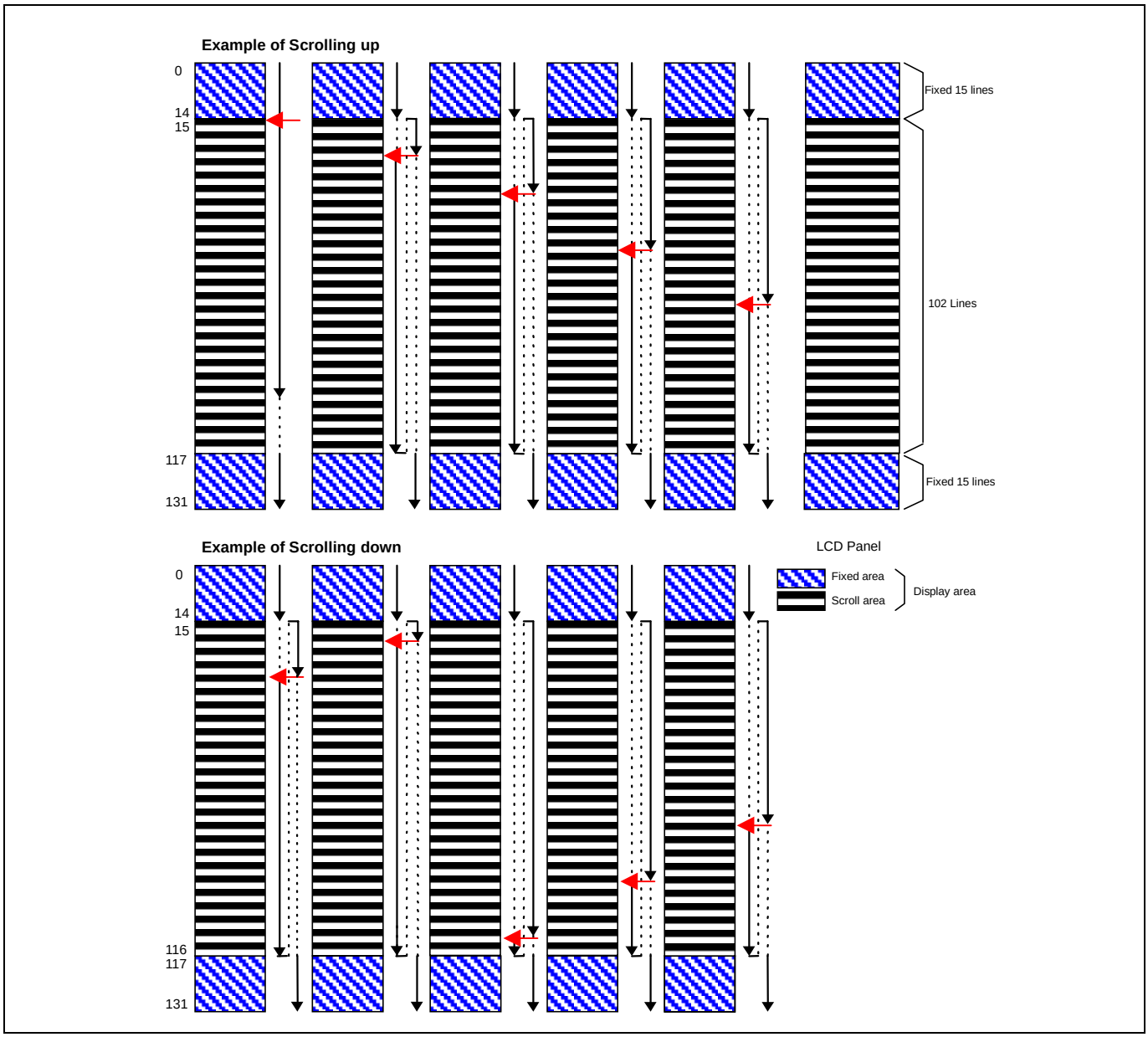
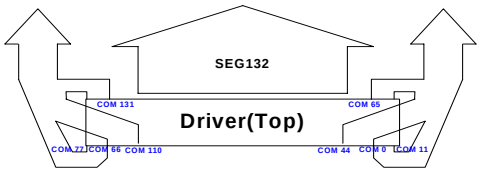


Figure 16. Area scroll examples (duty = 1/132, center scroll mode)

Display Direction

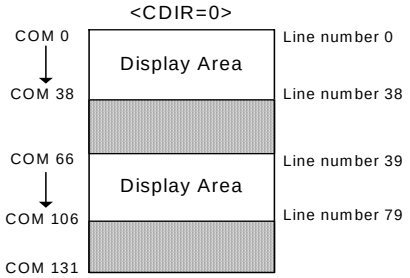
CDIR

The CDIR flag of Driver Output Mode Set Instruction selects the direction of common driver scanning.

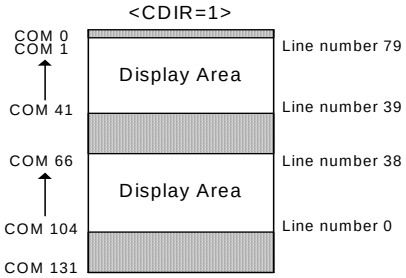


80 Display Lines (DLN=10)

<CDIR=0>

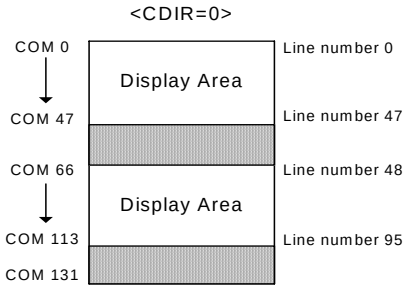


<CDIR=1>

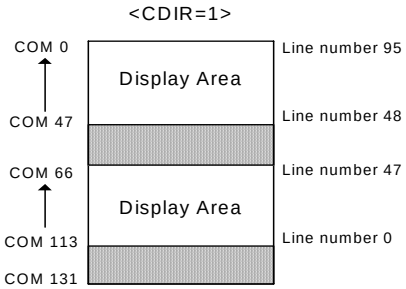


96 Display Lines (DLN=11)

<CDIR=0>

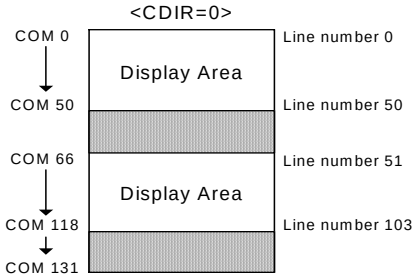


<CDIR=1>

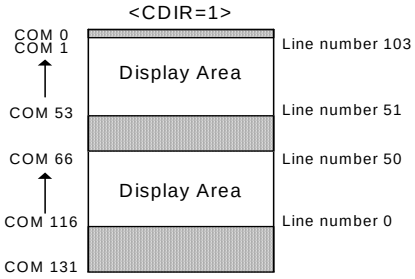


104 Display Lines (DLN=01)

<CDIR=0>

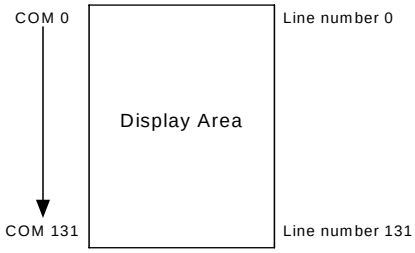


<CDIR=1>

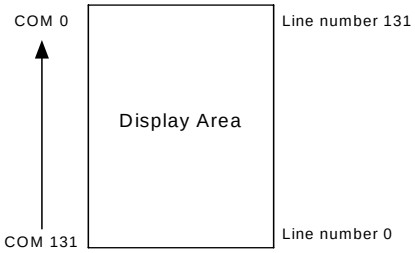


132 Display Lines (DLN=00)

<CDIR=0>

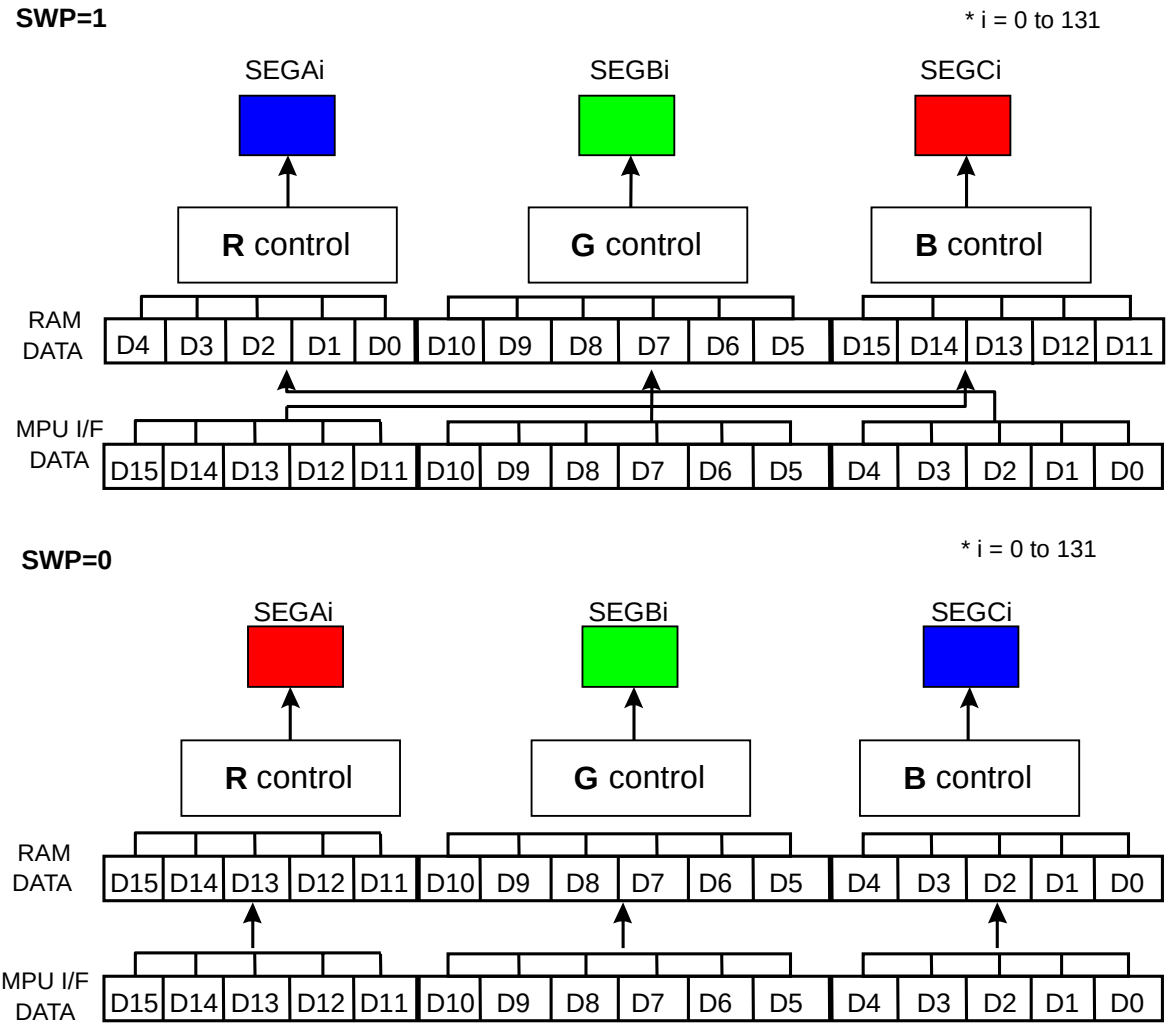


<CDIR=1>



SWP

The SWP flag of Driver Output Mode Set instruction selects the swapping of segment display.



	SEGAi	SEGBi	SEGCi	
SWP = 0	RED	GREEN	BLUE	Color
	D15 ~ D11	D10~ D5	D4 ~ D0	Assigned Bit
SWP = 1	BLUE	GREEN	RED	Color
	D4~ D0	D10 ~ D5	D15 ~ D11	Assigned Bit

Figure 17. The relationship between SEG outputs and RGB color

On-Chip Regulator Configuration

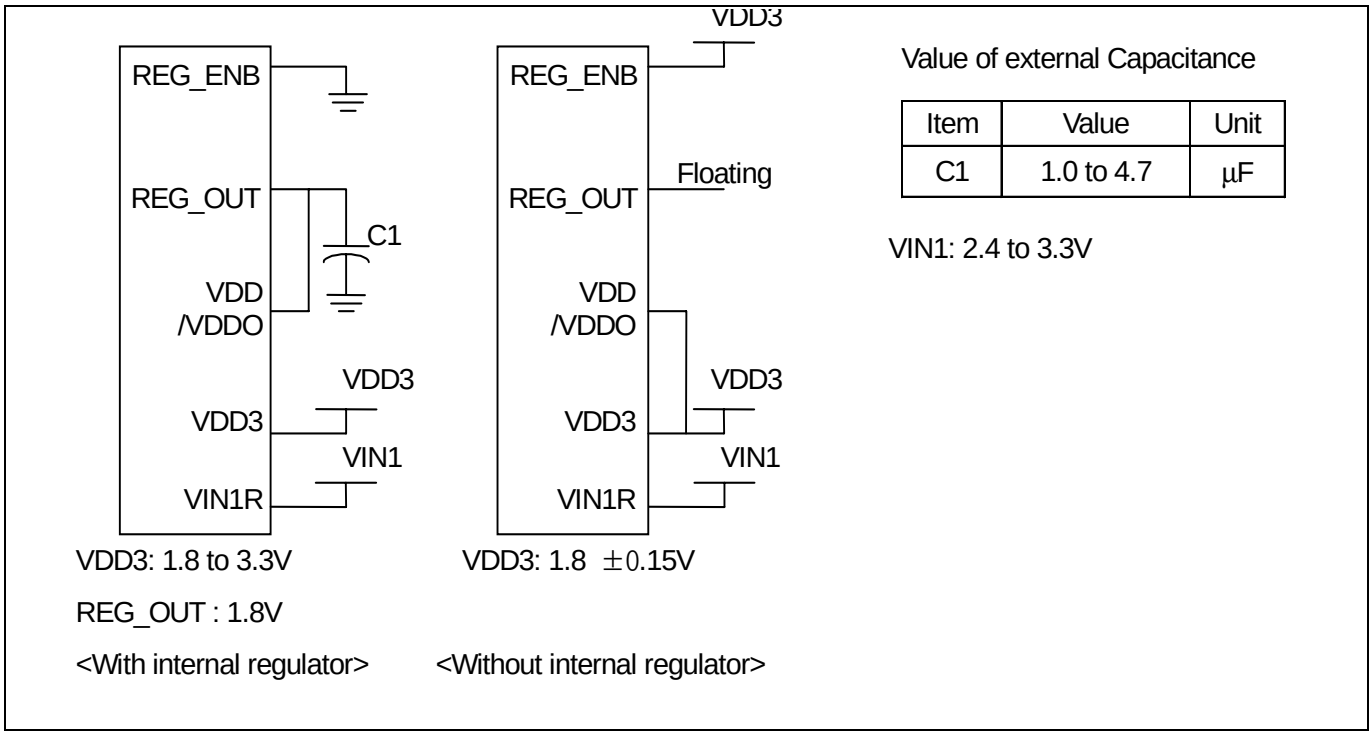


Figure 18. Regulator Application

Oscillator Circuit

When internal oscillator is used (EXT=0), the selection of oscillator resistor is determined by display mode.

- Normal display mode/Partial display mode 0 : resistor1 between OSC1 and OSC2
- Partial display mode 1 : resistor2 between OSC3 and OSC4

Note : In R-C oscillator, the oscillation frequency is changed according to the external resistance value, ITO wire length, or operating power-supply voltage(VDDO).

When external clock is used (EXT=1), clock frequency should be adjusted to display mode, which is selected.

Example of external oscillator application

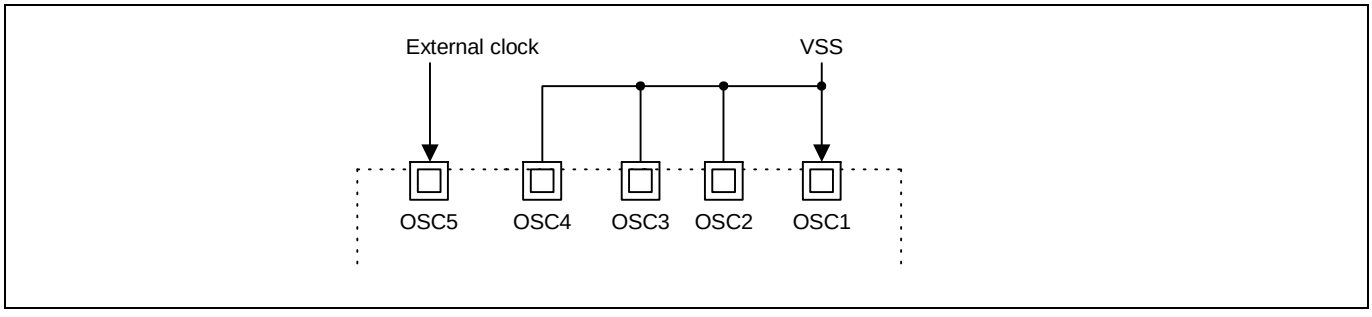
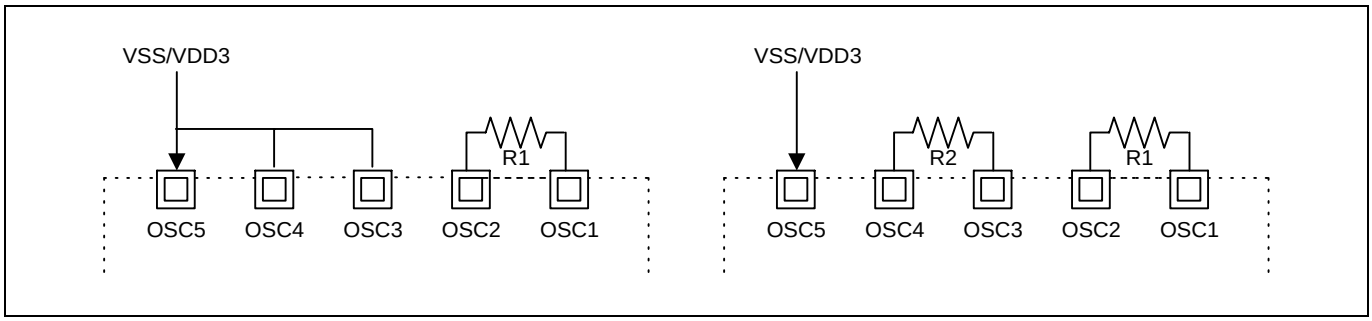


Figure 19. External oscillator application

Example of internal oscillator application

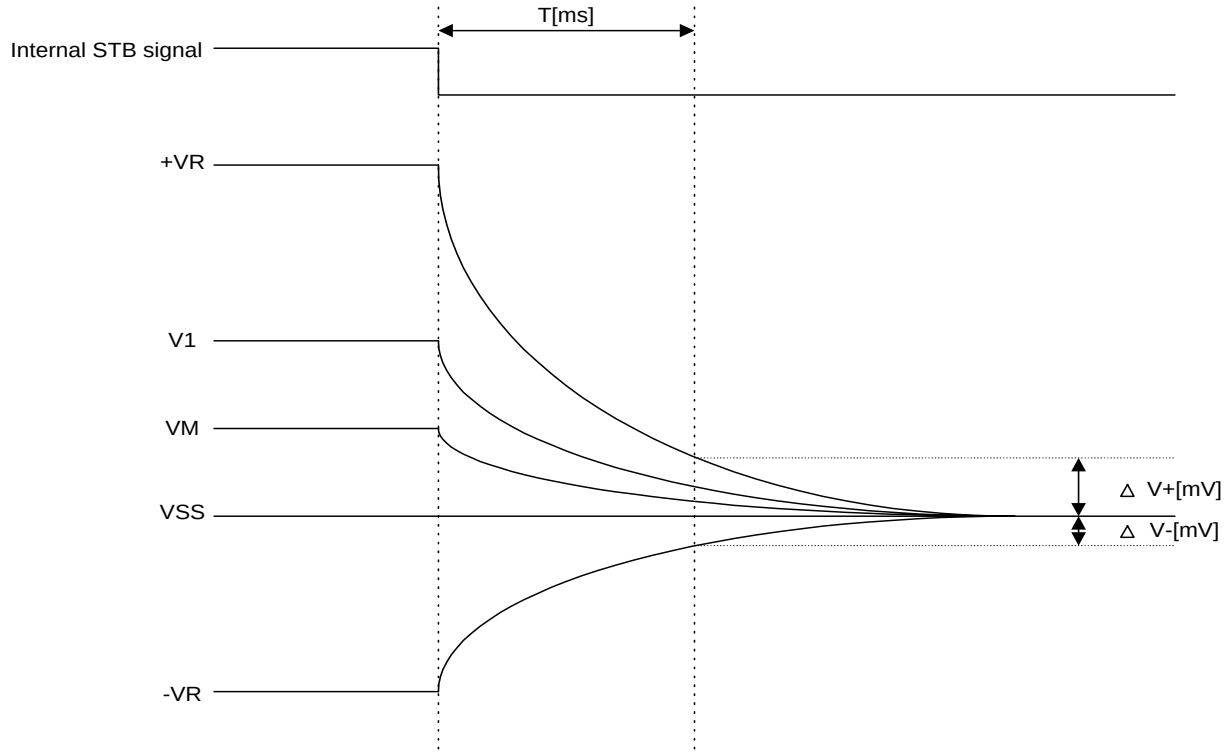


When normal/partial display mode 0 is used. When all display mode is used.

Figure 20. Internal oscillator application

Discharge Circuit

Driving voltage level discharge time at standby ON.



The relation between voltage level and discharge time from when “Standby ON” command is inputted.

LEVEL	CONDITION	T[ms]	ΔV+,ΔV-[mV]
+VR,V1,VM,-VR	+VR=12.0V, V1=3.0V, VM=1.5V, -VR=-9.0V at T=0	100	< 50
		300	< 20

INSTRUCTION DESCRIPTION

Table 20. Instruction Table

Instruction Name	D/I	WRB	RDB	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.	Parameter
Non Operation	0	0	1	*	0	0	0	0	0	0	0	0	00	
Oscillation Mode Set	0	0	1	*	0	0	0	0	0	0	1	0	02	1Byte
Driver Output Mode Set	0	0	1	*	0	0	0	1	0	0	0	0	10	1Byte
Monitor Signal Control	0	0	1	*	0	0	0	1	1	0	0	0	18	1Byte
DC-DC Select	0	0	1	*	0	0	1	0	0	0	0	0	20	1Byte
Bias Set	0	0	1	*	0	0	1	0	0	0	1	0	22	1Byte
DCDC Clock Division Set	0	0	1	*	0	0	1	0	0	1	0	0	24	1Byte
DCDC and AMP ON/OFF set	0	0	1	*	0	0	1	0	0	1	1	0	26	1Byte
Temperature Compensation Set	0	0	1	*	0	0	1	0	1	0	0	0	28	1Byte
Contrast Control(1)	0	0	1	*	0	0	1	0	1	0	1	0	2A	1Byte
Contrast Control(2)	0	0	1	*	0	0	1	0	1	0	1	1	2B	1Byte
Standby Mode OFF	0	0	1	*	0	0	1	0	1	1	0	0	2C	-
Standby Mode ON	0	0	1	*	0	0	1	0	1	1	0	1	2D	-
Addressing Mode Set	0	0	1	*	0	0	1	1	0	0	0	0	30	1Byte
ROW Vector Mode Set	0	0	1	*	0	0	1	1	0	0	1	0	32	1Byte
N-line Inversion Set	0	0	1	*	0	0	1	1	0	1	0	0	34	1Byte
Driving Mode Set	0	0	1	*	0	0	1	1	0	1	1	0	36	1Byte
Entry Mode Set	0	0	1	*	0	1	0	0	0	0	0	0	40	1Byte
Row address Area Set	0	0	1	*	0	1	0	0	0	0	1	0	42	2Byte
Column address Area Set	0	0	1	*	0	1	0	0	0	0	1	1	43	2Byte
RAM Skip Area Set	0	0	1	*	0	1	0	0	0	1	0	1	45	1Byte
Display OFF	0	0	1	*	0	1	0	1	0	0	0	0	50	-
Display ON	0	0	1	*	0	1	0	1	0	0	0	1	51	-
Specified Display Pattern Set	0	0	1	*	0	1	0	1	0	0	1	1	53	1Byte
Partial Display Mode Set	0	0	1	*	0	1	0	1	0	1	0	1	55	1Byte
Partial Display Start Line Set	0	0	1	*	0	1	0	1	0	1	1	0	56	1Byte
Partial Display End Line Set	0	0	1	*	0	1	0	1	0	1	1	1	57	1Byte
Area Scroll Mode Set	0	0	1	*	0	1	0	1	1	0	0	1	59	4Byte
Scroll Start Line Set	0	0	1	*	0	1	0	1	1	0	1	0	5A	1Byte
OTP Mode Off	0	0	1	*	1	1	1	0	1	0	1	0	EA	-
OTP Mode On	0	0	1	*	1	1	1	0	1	0	1	1	EB	-
Offset Volume Set	0	0	1	*	1	1	1	0	1	1	0	1	ED	1Byte
OTP Write Enable	0	0	1	*	1	1	1	0	1	1	1	1	EF	-
Display Data Write	1	0	1	Display Data Write									-	-
Display Data Read	1	1	0	Display Data Read									-	-
Status Read	0	1	0	*	Status Data Read								-	-

*: Don't care
Parameter: The number of parameter bytes that follows instruction data.

Non Operation (00H)

This instruction is Non operation.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0	0

Oscillation Mode Set (02H)

Setting internal function mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1	0
			0	0	0	0	0	0	EXT	OSC

EXT: External clock selecting
EXT = 0: Internal clock mode (Initial status)
EXT = 1: External clock mode

OSC: Internal oscillator ON/OFF
OSC = 0: Internal oscillator OFF(Initial status)
OSC = 1: Internal oscillator ON

Driver Output Mode Set (10H)

This instruction sets the display duty and direction.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0	0
			0	0	DLN		MY	MX	SWP	CDIR

DLN: Display Line Number selecting (DLN = 00 initial status)

DB5	DB4	Display Duty
0	0	1/132
0	1	1/104
1	0	1/80
1	1	1/96

MY: Selection Row Address Count.
MY = 0 : Row address increment (Initial status)
MY = 1 : Row address decrement

MX: Selection Column Address Count.
MX = 0 : Column address increment (Initial status)
MX = 1 : Column address decrement

SWP: Swap segment output SEGAi and SEGCi
This bit is for swapping the output of segment driver.
SWP = 0 (Initial status)

CDIR: Common Direction
This bit is for controlling the direction of common driver.
CDIR = 0 (Initial status)

Monitor Signal Control (18H)

This instruction configures the output enable and timing of monitor signal

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	1	0	0	0
			0	0	SYNSEL		SYNC	PM	CL	FR

SYNSEL : SYNC signal output timing selection (When Initial status, SYNSEL = “00”)

DB5	DB4	SYNC signal output timing
0	0	Head of 1st sub frame
0	1	Head of 2nd sub frame
1	0	Head of 3rd sub frame
1	1	Head of 4th sub frame

SYNC: Enable to transfer frame signal to output pin by active high
SYNC = 0 (Initial status)

PM: Enable to transfer field delimiter signal to output pin by active high
PM = 0 (Initial status)

CL: Enable to transfer shift signal to output pin by active high
CL = 0 (Initial status)

FR: Enable to transfer liquid crystal alternating signal to output pin by active high
FR = 0 (Initial status)

DC-DC Select (20H)

Selects DC-DC step-up of the common driver in normal and partial mode 0 and partial mode 1

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	0	0
			0	0	0	0	0	DC (2)	0	DC(1)

DC (2) : In partial mode 1	
DB2	DC-DC step up
0	X1.0
1	X1.5

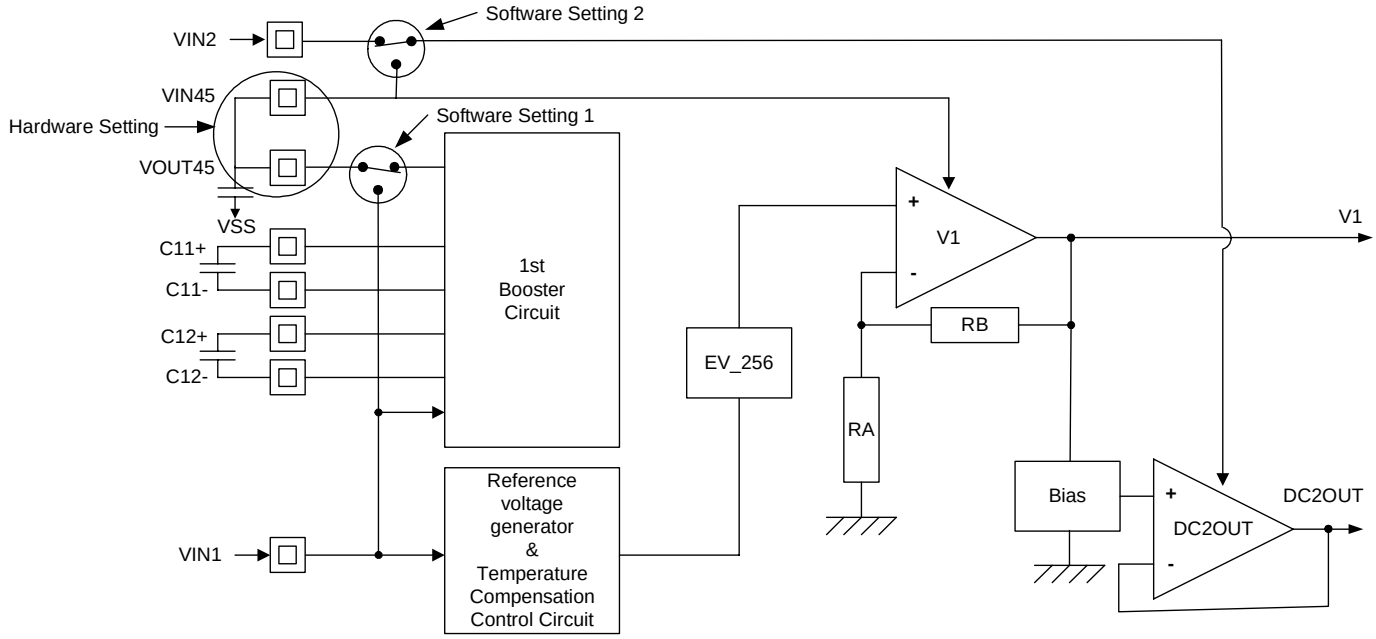
DC (1) : In normal mode, partial mode 0	
DB0	DC-DC step up
0	X1.0
1	X1.5

DC-DC Select and power supply for V1 Op-Amp.

Even if VIN45 is connected to VOUT45 or VIN1, a setup by software must be able to be performed.
Power supply for V1 Op-Amplifier is decided by hardware and instruction (20H) setting.
Power supply for DC2OUT Op-Amplifier is decided by software setting.

The example of usage is shown below.

Figure28. Example : Hardware Setting : VIN45 connected to VOUT45
Software Setting 1 : Power supply for V1 Op.Amp. uses 1'st booster output (not VIN1).
Software Setting 2 : Power supply for DC2OUT Op.Amp. uses VIN2 (not VIN45).



Hardware setting: VIN45 connected to (1) VOUT45 (when VOUT45 is used)
(2) VIN1 (when VOUT45 is not used)

Instruction setting: DC-DC Select (20H) - DC Register
Set value “0” Power supply for 1’st booster output uses 1XVIN1. (Initial status)
Set value “1” Power supply for 1’st booster output uses 1.5XVIN1.

Software setting 1: DC/DC and AMP ON/OFF (26H) – DCDC1 Register
Set value “0” Power supply for VOUT45 uses VIN1. (Initial status)
Set value “1” Power supply for VOUT45 uses 1’st booster output.

Software setting 2: DC/DC and AMP ON/OFF (26H) - VIN2 Register
Set value “0” Power supply for DC2OUT Op-Amp uses VIN2. (Initial status)
Set value “1” Power supply for DC2OUT Op-Amp uses VIN45.

Bias Set (22H)

This instruction set up the value of bias in normal mode and in partial mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	1	0
			0	0	Bias(2)		0	0	Bias(1)	

Bias(2): In partial mode 1				
DB5	DB4	Bias	DCDC2 step up	DC2OUT
0	0	1/4	X(-3)	3/4xV1
0	1	1/5	X(-4)	4/6xV1
1	0	1/6	X(-4)	5/6xV1
1	1	1/5	X(-3)	V1

Bias(1):In normal, partial mode 0				
DB1	DB0	Bias	DCDC2 step up	DC2OUT
0	0	1/4	X(-3)	3/4xV1
0	1	1/5	X(-4)	4/6xV1
1	0	1/6	X(-4)	5/6xV1
1	1	1/5	X(-3)	V1

DCDC Clock Division Set(24H)

This instruction sets the internal booster clock frequency.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	0	0
			DIV(2)				DIV(1)			

DIV : DC-DC Charge Pump Division Ratio in Normal Mode Display and Partial Display Mode
- DIV(1) = 0000 (Initial status)
- DIV(2) = 0000 (Initial status)

DIV(2):In partial mode 1				
DB7	DB6	DB5	DB4	fPCK
0	0	0	0	fOSC/8
0	0	0	1	fOSC/10
0	0	1	0	fOSC/12
0	0	1	1	fOSC/14
0	1	0	0	fOSC/16
0	1	0	1	fOSC/18
0	1	1	0	fOSC/20
0	1	1	1	fOSC/22
1	0	0	0	fOSC/24
1	0	0	1	fOSC/26
1	0	1	0	fOSC/28
1	0	1	1	fOSC/30
1	1	0	0	fOSC/32
1	1	0	1	fOSC/34
1	1	1	0	fOSC/36
1	1	1	1	fOSC/38

DIV(1):In normal, partial mode 0				
DB3	DB2	DB1	DB0	fPCK
0	0	0	0	fOSC/32
0	0	0	1	fOSC/36
0	0	1	0	fOSC/40
0	0	1	1	fOSC/44
0	1	0	0	fOSC/48
0	1	0	1	fOSC/52
0	1	1	0	fOSC/56
0	1	1	1	fOSC/60
1	0	0	0	fOSC/64
1	0	0	1	fOSC/68
1	0	1	0	fOSC/72
1	0	1	1	fOSC/76
1	1	0	0	fOSC/80
1	1	0	1	fOSC/84
1	1	1	0	fOSC/88
1	1	1	1	fOSC/92

Note: fOSC = (ROUNDUP (Duty/3) + dummy) x 4 x 31 x frame frequency

DC/DC and AMP ON/OFF Set (26H)

This instruction set up the DC/DC and Op-amp in common start up setting.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	1	0
			0	0	0	VIN2	AMP	DCDC3	DCDC2	DCDC1

VIN2: Software Switch to select the power of DC2 Op-amp
- -VIN2=0: The power of DC2 Op-amp is connected VIN2. (Initial status)
- -VIN2=1: The power of DC2 Op-amp is connected VIN45.

AMP: Built-in OP-AMP ON/OFF.
- AMP=0: OP-AMP OFF (Initial status)
- AMP=1: OP-AMP ON

DCDC1: Built-in 1'st Booster ON/OFF
- DCDC1= 0: 1'st Booster OFF (Initial status)
- DCDC1= 1: 1'st Booster ON

DCDC2: Built-in 2'nd Booster ON/OFF
- DCDC2= 0: 2'nd Booster OFF (Initial status)
- DCDC2= 1: 2'nd Booster ON

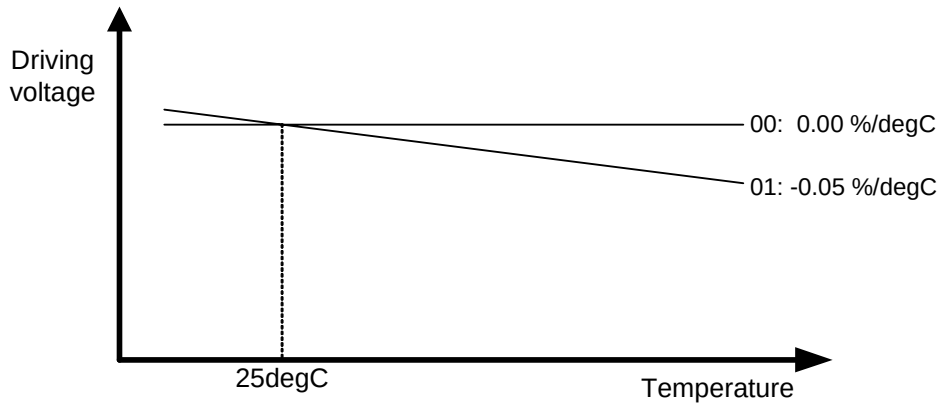
DCDC3: Built-in 3'rd Booster ON/OFF
- DCDC3= 0: 3'rd Booster OFF (Initial status)
- DCDC3= 1: 3'rd Booster ON

Temperature Compensation Set (28H)

This Instruction sets up the driving voltage slope for temperature compensation.

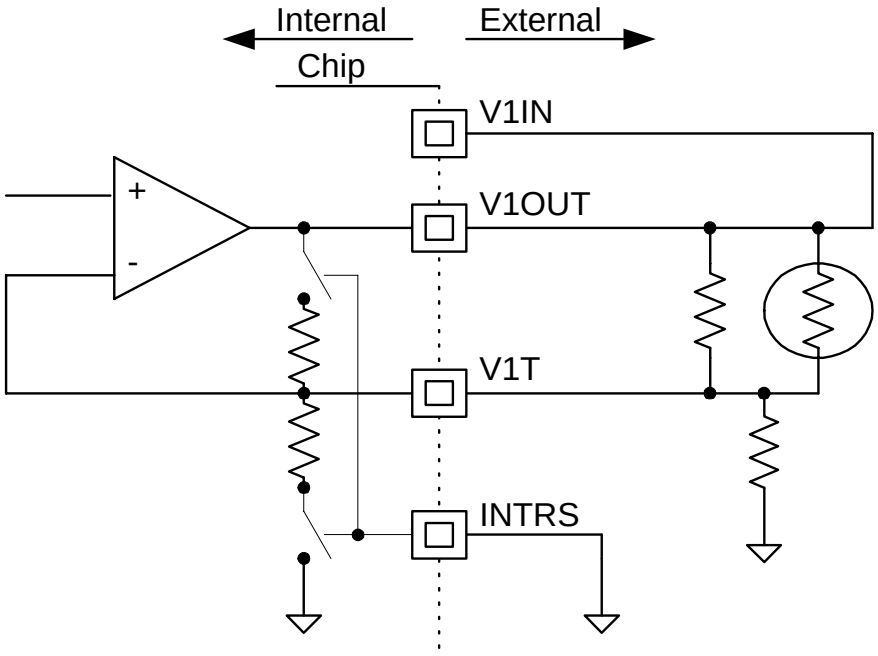
D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	0	0
			0	0	0	0	0	0	0	TCS

TCS: Temperature compensation slope set
- TCS = 0 : 0.00%/degC (Initial status)
- TCS = 1 : -0.05%/degC



Temperature Compensation

If external temperature compensation is needed, circuit diagram is described as below.
To use temperature compensation, two resistors and one thermistor are needed.



Contrast Control(1) (2AH)

This instruction updates the contrast control value in normal display mode and partial display mode 0.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	1	0
			Contrast control value (0 to 255)							

The relation between V1 voltage (typ.) and Contrast set value (8 step case)

Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]
00h	2.000	30h	2.376	60h	2.753	90h	3.129	C0h	3.506	F0h	3.882
08h	2.063	38h	2.439	68h	2.816	98h	3.192	C8h	3.569	F8h	3.945
10h	2.125	40h	2.502	70h	2.878	A0h	3.255	D0h	3.631	FFh	4.000
18h	2.188	48h	2.565	78h	2.941	A8h	3.318	D8h	3.694		
20h	2.251	50h	2.627	80h	3.004	B0h	3.380	E0h	3.757		
28h	2.314	58h	2.690	88h	3.067	B8h	3.443	E8h	3.820		

Contrast Control(2) (2BH)

This instruction updates the contrast control value in partial display mode 1.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	1	1
			Contrast control value (0 to 255)							

The relation between V1 voltage (typ.) and Contrast set value (8 step case)

Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]
00h	2.000	30h	2.376	60h	2.753	90h	3.129	C0h	3.506	F0h	3.882
08h	2.063	38h	2.439	68h	2.816	98h	3.192	C8h	3.569	F8h	3.945
10h	2.125	40h	2.502	70h	2.878	A0h	3.255	D0h	3.631	FFh	4.000
18h	2.188	48h	2.565	78h	2.941	A8h	3.318	D8h	3.694		
20h	2.251	50h	2.627	80h	3.004	B0h	3.380	E0h	3.757		
28h	2.314	58h	2.690	88h	3.067	B8h	3.443	E8h	3.820		

Note :
S6B33B3 has a hardware protection for "2VR < 20V". It means the limitation of contrast value in 1/6 bias.
If 1/6 bias is set, max contrast value is limited to A9h.

Standby Mode OFF (2CH)

This instruction releases the standby mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	0

The internal statuses during standby off are as following:

- All commons output: +VR or –VR or VM
- All segments output: VSS or V1
- Oscillator circuit: On (EXT = 0, OSC=1),OFF (others)
- Displaying clocks (FR, PM, CL, SYNC): In operation

Function and Pin condition at standby OFF

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON(Operate)
COM outputs	+VR or VM or -VR
SEG outputs	V1 or VSS or VM

Standby Mode ON (2DH)

This instruction enters the standby mode to reduce the power consumption to the static power consumption value (Initial status). The following instructions, standby off and display on, cause returning to the normal operation status.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	1

The internal statuses during standby on are as following:

- All common and segment output: VSS
- Oscillator circuit: OFF
- Displaying clocks (FR, PM, CL, SYNC) are held.

Function and Pin condition at standby ON

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	OFF
SEG and COM outputs	VSS

LCD driving power output condition at Standby ON.

level	Condition
+VR	VSS
V1	VSS
VM	VSS
-VR	VSS

Addressing Mode Set (30H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	0	0
			FIR	0	GSM	DSG	SGF	0	SGP	0

FIR : frame inversion relationship between PWM phase and Row polarity
- 0 : Case1 (Initial status)
- 1 : Case2

Frame		0	1	2	3
PWM phase in 1st subgroup (SGP = 0)					
Row polarity (FIM = 1)	Case1	Normal	Reverse	Normal	Reverse
	Case2	Reverse	Normal	Reverse	Normal

GSM: Gray Scale Mode
- 0: 65,536 color mode (Initial status)
- 1: 4,096 color mode

DSG : Duty Adjust Setting
- 0 : Dummy subgroup is one subgroup (Initial status)
- 1 : Dummy subgroup is none

SGF : Sub Group Frame Inversion mode setting
- 0: SG Frame inversion OFF (Initial status)
- 1: SG Frame inversion ON

SGP : Sub Group Phase mode setting
- 0 : Same phase in all pixels (Initial status)
- 1 : Different phase by 1pixel-unit

Row Vector Mode Set (32H)

Setting ROW function.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	1	0
			0	0	0	0	INC			VEC

INC: Row Vector Increment Mode. This Parameter set up Row vector increment period

DB3	DB2	DB1	Row Vector Increment Period
0	0	0	Every subgroup
0	0	1	Every 2subgroup
0	1	0	Every 4subgroup
0	1	1	Every 8subgroup
1	0	0	Every 16subgroup
1	0	1	Every 16subgroup
1	1	0	Every 16subgroup
1	1	1	Every subframe (Initial status)

VEC: ROW Vector Sequence Mode
- 0: R0->R1->R2->R3 -> R0… (Initial status)
- 1: R0->R1->R2->R3->R0->R1->R2->R3… (when N frame)
  R4->R5->R6->R7->R4->R5->R6->R7… (when N+1 frame)

3X4 Row Function

	R0	R1	R2	R3
L0	0	1	1	1
L1	1	0	1	1
L2	1	1	0	1

3X8 Row Function

	R0	R1	R2	R3	R4	R5	R6	R7
L0	0	1	1	1	1	1	0	1
L1	1	0	1	1	1	0	1	1
L2	1	1	0	1	0	1	1	1

Note: 1 represents VRP, 0 represents VRN

N-block inversion Set (34H)

This instruction set up N block inversion for AC driving.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	0	0
			FIM	0	0	N-block inversion				

FIM: Forcing Inversion Mode
FIM = 0: Forcing Inversion OFF (Initial status)
FIM = 1: Forcing Inversion ON

N-block Inversion : This parameter indicates the basic period of polarity inversion. (Initial status = 0Dh)
The whole period of polarity inversion is decided by FIM and this parameter.

DB7	DB6	DB5	DB4 – DB0	Polarity Inversion Period
X	X	X	0	every frame
0	X	X	1	every 1 block
:	:	:	:	:
0	X	X	31	every 31 blocks
1	X	X	1	every 1 block and every frame
:	:	:	:	:
1	X	X	31	every 31 blocks and every frame

Driving Mode Set (36H)

This instruction controls the internal driving mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	1	0
			0	0	SPT	0	SCS	CC	CCM	LFS

SPT: Selection Pulse Type.
SPT = 0 : Equally Distributed MLA (Initial status)
SPT = 1 : Partially Distributed MLA

Note: The following instructions (SCS/CC/CCM) don't operate in Partially Distributed MLA.
VEC forcibly becomes VEC = 0

SCS: Segment Charge Share.
SCS = 0 : Segment charge share is invalid (Initial status)
SCS = 1 : Segment charge share is valid

CC: Cross-talk Compensation.
CC = 0 : Cross-talk compensation is invalid(Initial status)
CC = 1 : Cross-talk compensation is valid

CCM: Cross-talk Compensation Mode.
CCM = 0 : The coefficient of cross-talk compensation is 1/4 (Initial status)
CCM = 1 : The coefficient of cross-talk compensation is 1/8

LFS: Low frame frequency set for low power consumption.
LFS = 0 : Low frequency set OFF (Initial status)
LFS = 1 : Low frequency set ON

Note: fFR @(LFS=1) = fFR @(LFS=0) / 2

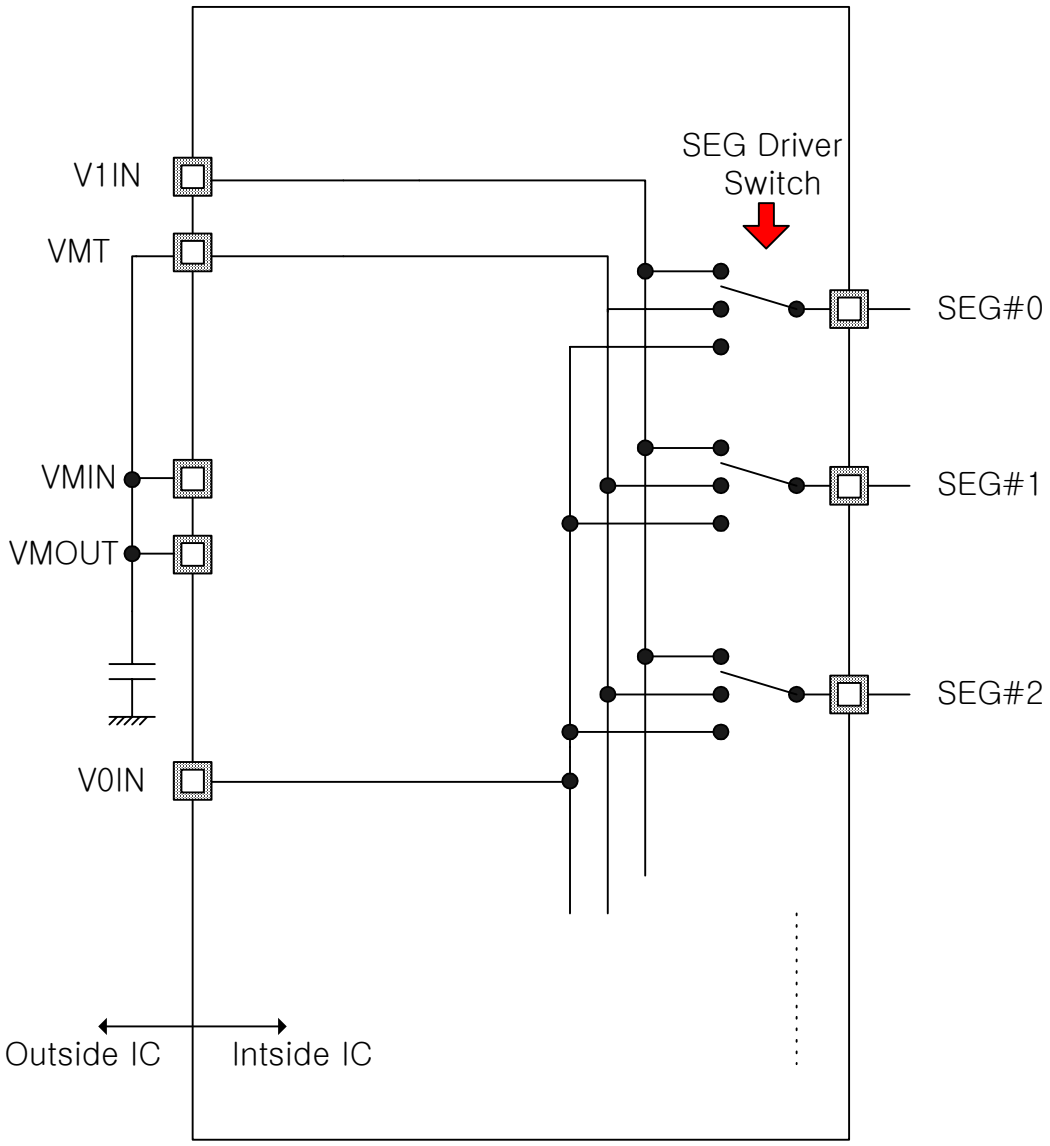


Figure 21.Segment Charge Sharing Circuit for SEG Driver

Note) C-tank and VMIN/VMOUT are connected outside IC

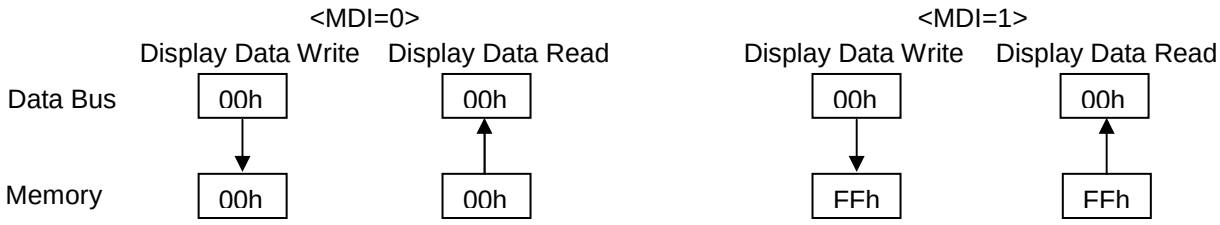
Entry Mode Set (40H)

Setting internal function mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0	0
			16B	0	0	0	0	MDI	Y/X	RMW

16B: Selection data bus width.
16B = 0 : 16bit data bus (Initial status)
16B = 1 : 8bit data bus

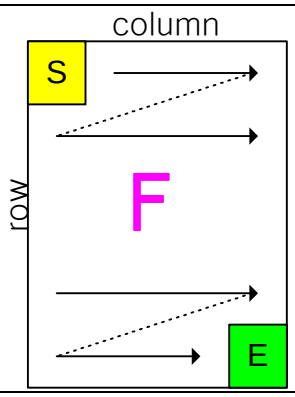
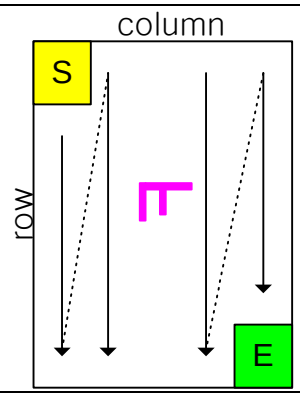
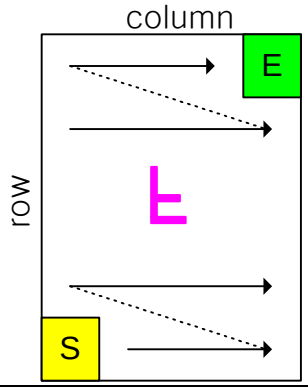
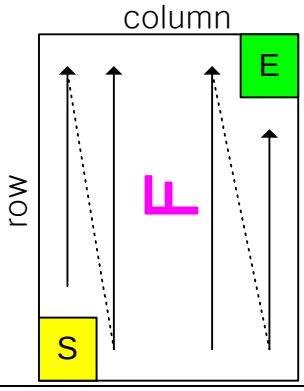
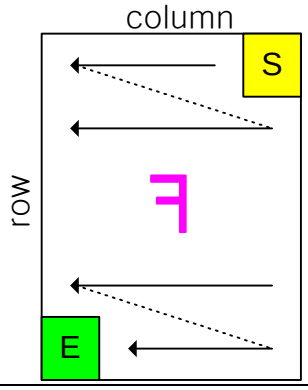
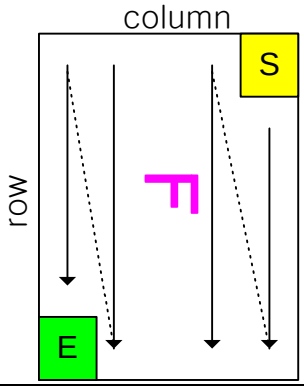
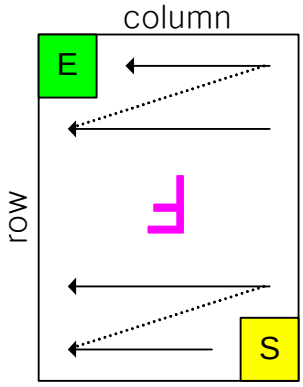
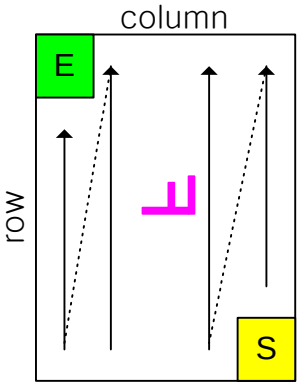
MDI: Memory data inversion setting for low power consumption.
MDI = 0: Memory data inversion OFF (Initial status)
MDI = 1: Memory data inversion ON



Y/X: Selection Address Count.
Y/X = 0 : Column address count first (Initial status)
Y/X = 1 : Row address count first

RMW: Read modify write mode ON/OFF select
RMW = 0: Read modify write OFF (Initial status)
RMW = 1: Read modify write ON. When this mode is on, X(Y) address of on-chip display RAM is not increment in reading display data but in writing display data.

Table 21.Entry Mode Set Table

Display Data Direction	Entry Mode Set Y/X	MX	MY	Stored data into DDRAM	Display Data Direction	Entry Mode Set Y/X	MX	MY	Stored data into DDRAM
Normal	0	0	0		X-Y Exchange	1	0	0	
Y-Mirror	0	0	1		X-Y Exchange Y-Mirror	1	0	1	
X-Mirror	0	1	0		X-Y Exchange X-Mirror	1	1	0	
X-Mirror Y-Mirror	0	1	1		X-Y Exchange X-Mirror Y-Mirror	1	1	1	

Row Address Area Set (42H)

This instruction and parameter set up the Y address areas of the on-chip display data RAM.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	0
			Y start address set (Initial Status = 00H)							
			Y end address set (Initial Status = 83H)							

The current Y address of the on-chip display data RAM is the Y start address by setting this instruction. In Y address count mode (Y/X = “H”), the Y address is increased from Y start address to Y end address. When Y address is equal to the Y end address, the X address is increased by 1 and the Y address returns to Y start address. The Y start and Y end addresses must be set as a pair and Y start address must be less than Y end address.

Column Address Area Set (43H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	1
			X start address set (Initial Status = 00H)							
			X end address set (Initial Status = 83H)							

The current X address of the on-chip display data RAM is the X start address by setting this instruction. In X address count mode (Y/X = “L”), the X address is increased from X start address to X end address. When X address is equal to the X end address, the Y address is increased by 1 and the X address returns to X start address. The X start and X end address must be set as a pair and X start address must be less than X end address.

RAM Skip Area Set (45H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

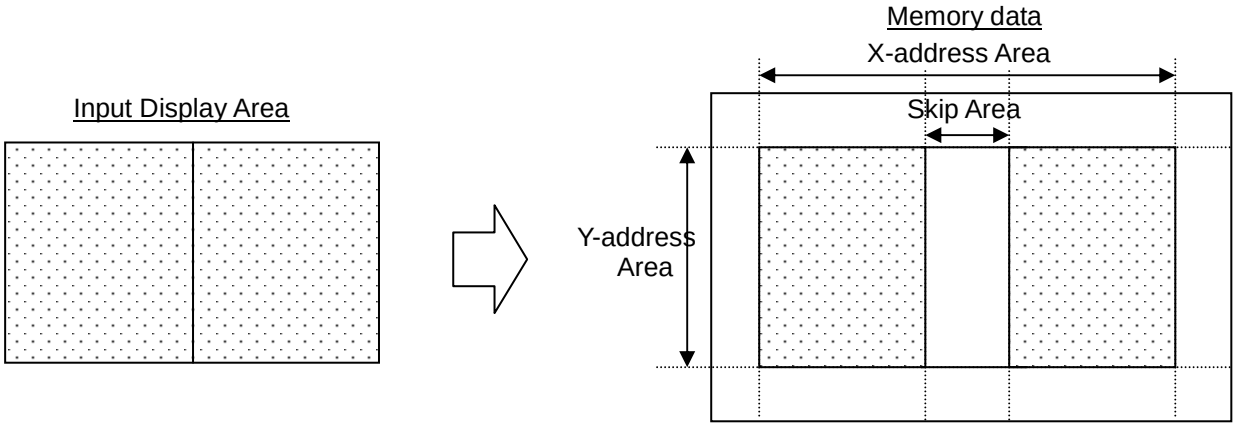
D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	0	1
			0	0	0	0	0	0	RSK	

RSK : RAM Skip function ON/OFF set

- RSK = 00 : No Skip (initial status)
- RSK = 01 : X address 34h-4Fh skip(104 RGB)
- RSK = 10 : X address 3Ch-47h skip(120 RGB)
- RSK = 11 : X address 30h-53h skip(96RGB)

RAM Skip Area Set

RAM Skip Area Set can skip a part of RAM X-address area. After setting RAM skip area, X-address count skip this area and count. In other words, X address after skip area is changed into X address which added a part for skip area.



Display OFF (50H)

Turn the display OFF(Initial status).
When display is off, all segment and common output are VSS level.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	0

Function and Pin condition at Display OFF

Function/Pin	Condition
DC/DC booster (1'st,2'nd,3'rd)	ON(Operate)
SEG and COM outputs	VSS

Display ON (51H)

Turns the display ON.
In case of being standby mode, this instruction does not work. This instruction is executed after standby mode off.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1

Function and Pin condition at Display ON

Function/Pin	Condition
DC/DC booster (1'st,2'nd,3'rd)	ON(Operate)
COM outputs	+VR or VM or -VR
SEG outputs	V1 or VSS or VM

Specified Display Pattern Set (53H)

This instruction sets the specified display pattern.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	1	1
			0	0	0	0	0	0	SDP	

SDP : Specified Display Pattern set

- SDP = 00 : Normal display
- SDP = 01 : Reverse display : Display data reversing mode setting without the contents of the display RAM
- SDP = 10 : Whole display pattern becomes OFF regardless of the RAM data.
- SDP = 11 : Whole display pattern becomes ON regardless of the RAM data.

Partial Display Mode Set (55H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	0	1
			0	0	0	0	0	PDTY	PDM	PT

DB0	DB1	DB2	Display Mode	Duty
PT	PDM	PDTY		
0	X	X	Normal	depend on DLN
1	0	X	Partial 0	
1	1	0	Partial 1	1/66
1	1	1		1/36

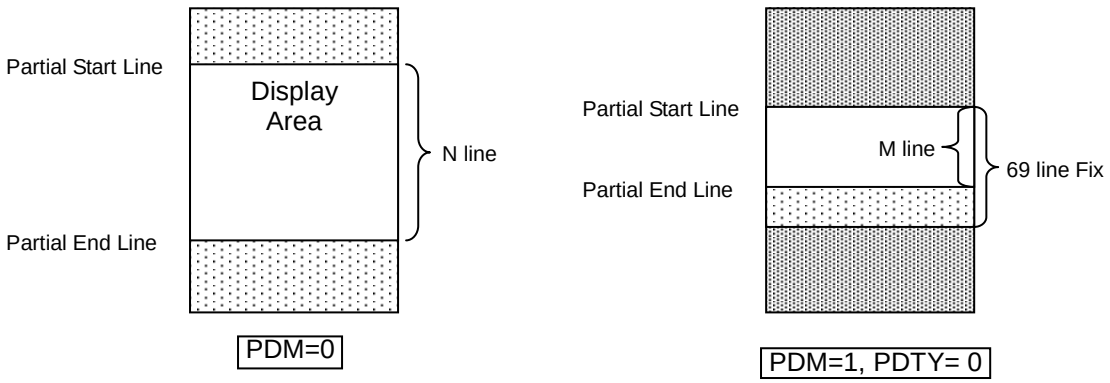
PT: Partial Display ON/OFF
- PT = 0: Partial display OFF = Normal mode (Initial status)
- PT = 1: Partial display ON

PDM: Partial Display mode set
- PDM = 0: Partial mode 0 : Duty ratio is same as Normal display mode(initial status)
- PDM = 1: Partial mode 1 : Duty ratio is changed from Normal display mode

PDTY: Duty selection
- PDTY = 0 (DSG = 0 : 69 line fixed(including 1 dummy subgroup),
  DSG = 1 : 66 line fixed(no dummy subgroup))
- PDTY = 1 (DSG = 0 : 39 line fixed(including 1 dummy subgroup),
  DSG = 1 : 36 line fixed(no dummy subgroup))

Applied parameter in PDM and PDTY are summarized as below

PDM	PDTY	Contrast	Duty	Bias	DC-DC Select	OSC	PCK
0	X	Contrast control(1)	Normal	Bias(1)	DC(1)	OSC1-OSC2	DIV(1)
1	0	Contrast control(2)	1/69	Bias(2)	DC(2)	OSC3-OSC4	DIV(2)
	1		1/39				



No display Area : No COM Scanning field (COM = VM fixed)

Except Partial Display Area : COM Timing is existing, but COM = VM fixed

Partial Display Area : Real display field

Operation in Partial Display Mode 0 (PDM=0)

On scanning except partial display area
- SEG output select V0 or V1 level depends on “FR” value. Refer to Figure 24.
- All of COM output is fixed VM level.

On scanning partial display area
- It is equal to be in normal mode

Operation in Partial Display Mode 1 (PDM=1, PDTY)

Display area is from partial start line to partial end line.
(COM driver output is fixed VM except display area, only max69 line output COM signal.
On scanning except partial display area
- SEG output select V0 or V1 level depends on “FR” value. Refer to Figure 24.
- All of COM output is fixed VM level.

Partial Display Mode 0

Item	Partial Display Area	Out of Partial Display Area
Duty	Same as normal display mode	
Bias	Same as normal display mode (Bias(1) setting)	
Contrast	Same as normal display mode (Contrast(1) setting)	
Oscillator	Same as normal display mode (OSC1 – OSC2)	
SEG Output level	Same as normal mode (V1,V0)	Depends on Internal “FR” signal See Figure 24
COM Output level	Same as normal mode (+VR,VM,-VR)	VM fixed

Partial display mode1

Item	Partial Display Area	Out of Partial Display Area	Out of Display Area
Duty	1/69 or 1/39 duty		
Bias	Bias(2) setting		
Contrast	Contrast(2) setting		
Oscillator	(OSC3 – OSC4) setting value		
SEG Output level	Same as normal mode (V1,V0)	Depends on “FR” signal See Figure 24	-
COM Output level	Same as normal mode (+VR, VM, -VR)	VM fixed	VM fixed

In case of COM 6 to COM11 Partial display

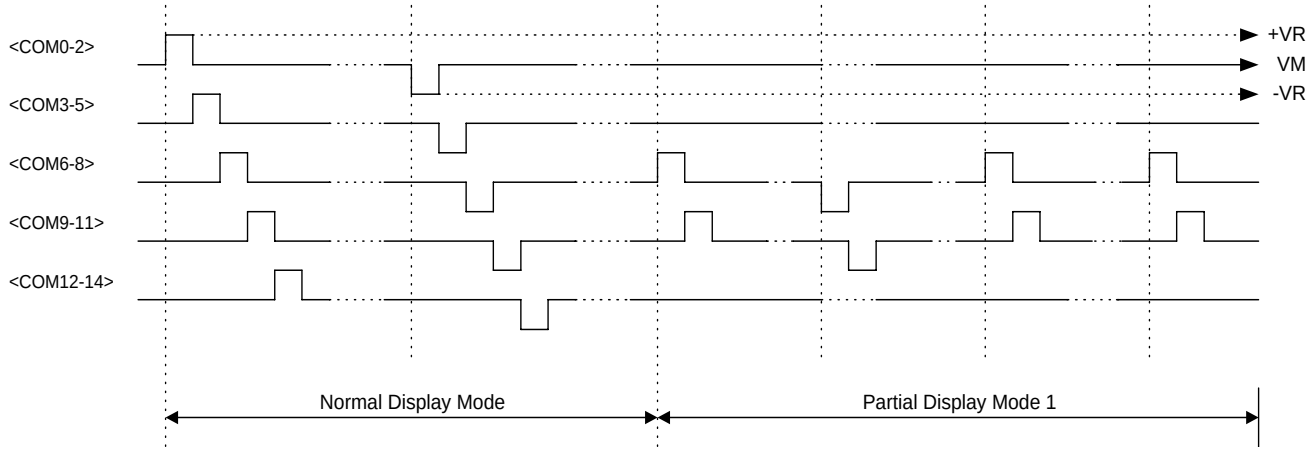


Figure 22.COM Waveform of Normal and Partial mode 1

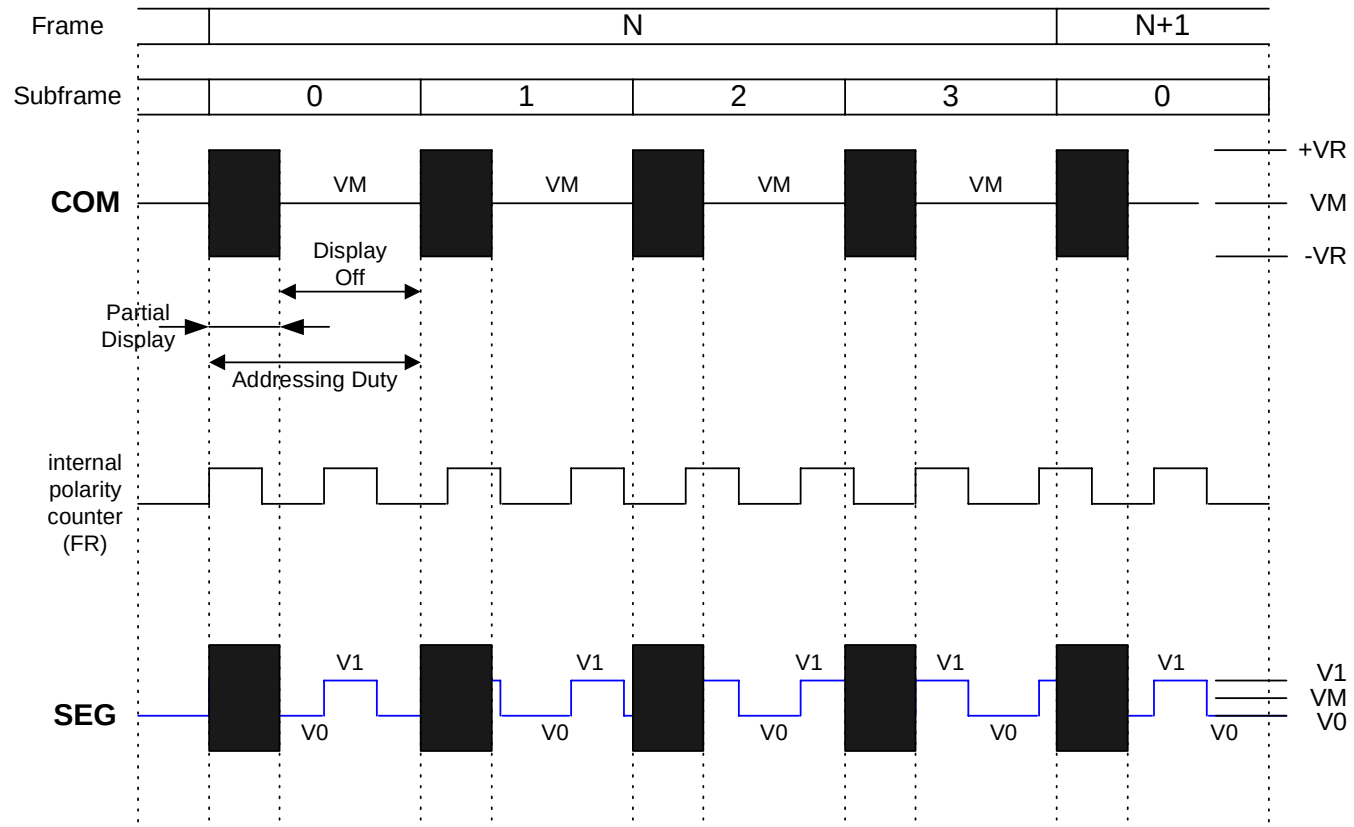


Figure 23.Example of Segment Voltage in non-display area

Partial Display Start Line Set (56H), Partial Display End Line Set(57H)

These 2 instructions set the partial display area and it is possible to display a part.

Partial Display Start Line Set (56H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	0
			Partial start line							

Partial Display End Line Set (57H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	1
			Partial end line							

COM 0	line 0
COM 1	line 1
COM 2	line 2
COM 3	line 3
	:
	:
	:
COM 128	line 128
COM 129	line 129
COM 130	line 130
COM 131	line 131

Parameter set appoints display line number. Parameter Size is able to be in a number of Display lines. Partial end line must set bigger number than Partial start line.

Area scroll Set (59H)

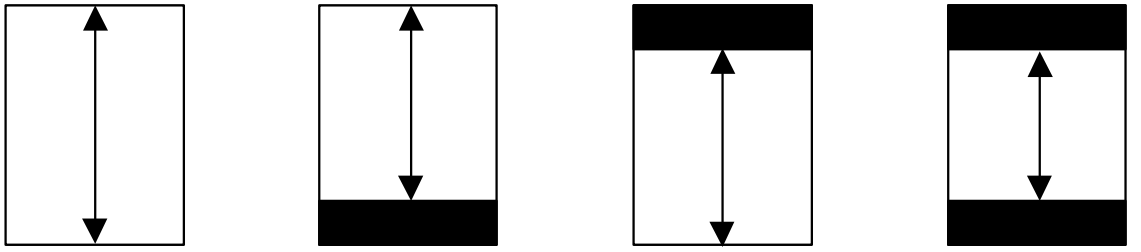
This instruction sets up area scroll field (start line, end line, Lower fixed line number), and it is possible to make screen to display as partial scroll field.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	0	1
			0	0	0	0	0	0	SCM	
			0	Scroll area start line						
			0	Scroll area end line						
			0	Lower fixed number						

Note: In lower and center scroll mode, scroll area end line must be smaller than (duty - lower fixed number).

SCM: Scroll mode setting

DB1	DB0	Mode
0	0	Entire display (Initial status)
0	1	Upper scroll display
1	0	Lower scroll display
1	1	Center scroll display



Entire Display Upper Display Lower Display Center Display

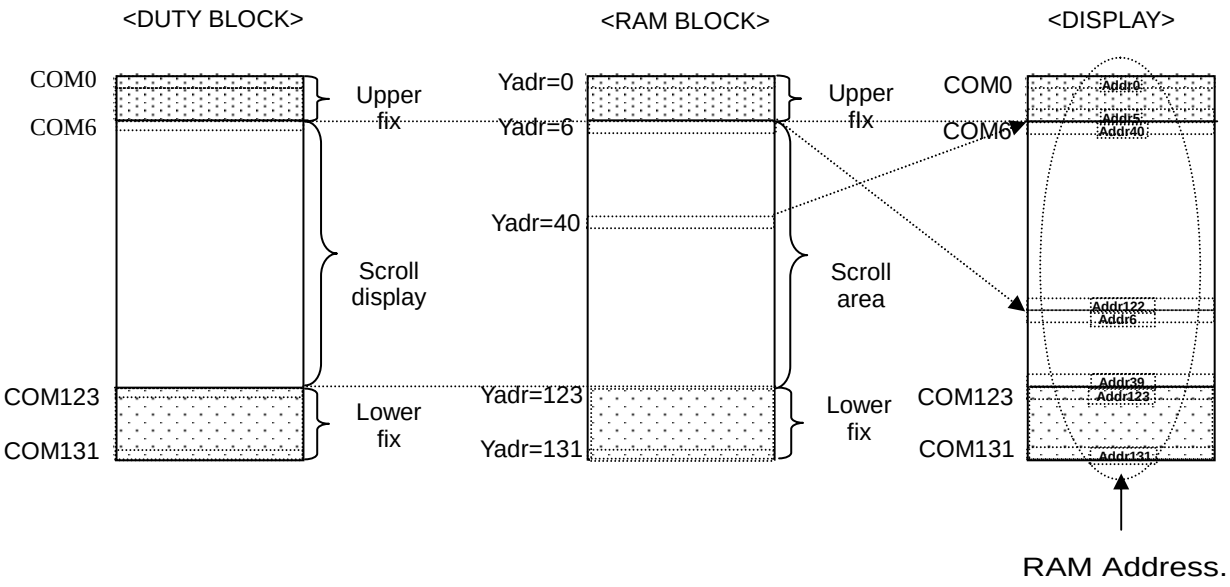
Scroll Start Line Set (5AH)

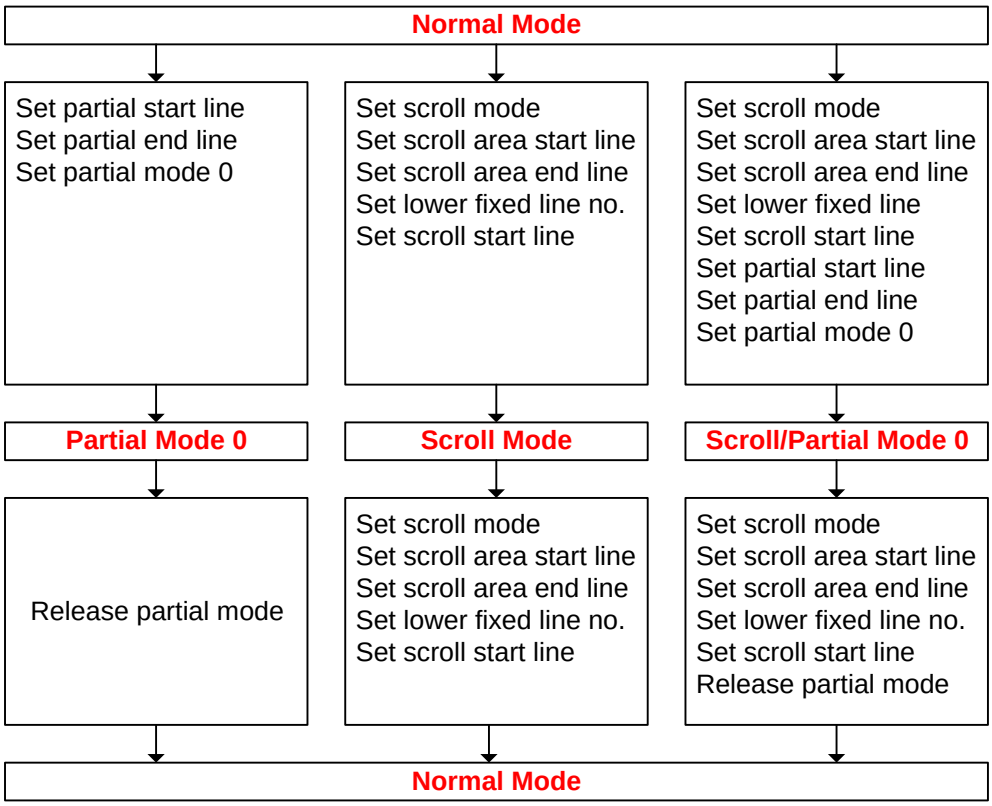
This instruction and parameter set up scroll start line. On this instruction, scroll start line becomes the first of area scroll field. Scroll operation is occurred every issue of this instruction.

D/I	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	1	0
			0	Scroll start line						

<Example>

-DLN : 2'b00 (1/132 Duty)
-SCM : 2'b11 (Center display mode)
-Scroll area start line : 6
-Scroll area end line : 122
-Lower fixed number : 9
-Scroll start line : 40


<DUTY BLOCK>
<RAM BLOCK>
<DISPLAY>
COM0
COM6
COM123
COM131
Upper fix
Scroll display
Lower fix
Yadr=0
Yadr=6
Yadr=40
Yadr=123
Yadr=131
Upper fix
Scroll area
Lower fix
COM0
COM6
COM123
COM131
Addr0
Addr5
Addr40
Addr122
Addr6
Addr39
Addr123
Addr131
RAM Address.


Normal Mode
Set partial start line
Set partial end line
Set partial mode 0
Set scroll mode
Set scroll area start line
Set scroll area end line
Set lower fixed line no.
Set scroll start line
Set scroll mode
Set scroll area start line
Set scroll area end line
Set lower fixed line
Set scroll start line
Set partial start line
Set partial end line
Set partial mode 0
Partial Mode 0
Scroll Mode
Scroll/Partial Mode 0
Release partial mode
Set scroll mode
Set scroll area start line
Set scroll area end line
Set lower fixed line no.
Set scroll start line
Set scroll mode
Set scroll area start line
Set scroll area end line
Set lower fixed line no.
Set scroll start line
Release partial mode
Normal Mode

Display Data Write/Read

D/I	WRB	RDB	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	Display RAM write in data								
1	1	0	Display RAM read out data								

GSM = 0(65,536 Color Mode)

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
2'nd cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3
2'nd cycle	G2	G1	G0	B4	B3	B2	B1	B0
3'rd cycle	R4	R3	R2	R1	R0	G5	G4	G3
4'th cycle	G2	G1	G0	B4	B3	B2	B1	B0

GSM = 1(4,096 Color Mode)

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
2'nd cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0
2'nd cycle	G3	G2	G1	G0	B3	B2	B1	B0
3'rd cycle	X	X	X	X	R3	R2	R1	R0
4'th cycle	G3	G2	G1	G0	B3	B2	B1	B0

Status Read

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	BUSY	Y/X	OPRT	PDM	PT	STB	REV	DP

This instruction indicates the internal status of the S6B33B3.

DP: (0 : Display OFF Status, 1 : Display ON Status)
REV: (0 : Display Image Non-Reversing, 1 : Display Image Reversing)
STB: (0 : Standby Mode OFF Status, 1 : Standby Mode ON Status)
PT: (0 : Partial Display Mode OFF Status, 1 : Partial Display Mode ON Status)
PDM: (0 : Partial Display Mode 0, 1 : Partial Display Mode 1)
OPRT: (0: OTP mode non-protection status, 1: OTP mode protection status)
Y/X: (0 : X-address Count Mode, 1 : Y-address Count Mode)
BUSY: (0 : No Busy, 1 : Busy)

OTP Mode Off (EAH)

This command is used to turn OTP mode off.

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	0	1	0

OTP Mode On (EBH)

This command is used to turn OTP mode on. (Initial status)

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	0	1	1

Offset Volume Set (EDH)

This command is used to set offset value x (-32 to +31) to electronic volume by 2's complement.

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	0	1
0	0	0	0	P5	P4	P3	P2	P1	P0

P5	P4	P3	P2	P1	P0	Offset Volume
0	1	1	1	1	1	31
:	:	:	:	:	:	
0	0	0	0	0	1	1
0	0	0	0	0	0	0
1	1	1	1	1	1	-1
	:	:	:	:	:	:
1	0	0	0	0	0	-32

OTP Write Enable (EFH)

This command is used to write offset value (OV) into EPROM cells.

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	1

INSTRUCTION PARAMETER

Table 22.Instruction Parameter

Instruction	Hex	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Oscillation Mode Set	02H	1	LFS	0	0	0	0	0	EXT	OSC
			0	*	*	*	*	*	0	0
Driver Output Mode Set	10H	1	0	0	DLN		MY	MX	SWP	CDIR
			*	*	0	0	0	*	*	0
Monitor Signal control	18H	1	0	0	SYNSEL		SYNC	PM	CL	FR
			*	*	0	0	0	0	0	0
DC-DC Set	20H	1	0	0	0	0	0	DC(2)	0	DC(1)
			*	*	*	*	*	*	*	0
Bias Set	22H	1	0	0	Bias(2)		0	0	Bias(1)	
			*	*	0	0	*	*	0	0
DCDC Clock Division Set	24H	1	DIV(2)				DIV(1)			
			0	0	0	0	0	0	0	0
DCDC and AMP ON/OFF Set	26H	1	0	0	0	VIN2	AMP	DCDC3	DCDC2	DCDC1
			*	*	*	0	0	0	0	0
Temperature Compensation Set	28H	1	0	0	0	0	0	0	0	TCS
			*	*	*	*	*	*	*	0
Contrast Control (1)	2AH	1	Contrast control value in normal and partial display mode0(0 to 255)							
			0	0	0	0	0	0	0	0
Contrast Control (2)	2B	1	Contrast control value in partial display mode1(0 to 255)							
			0	0	0	0	0	0	0	0
Addressing Mode Set	30H	1	FIR	0	GSM	DSG	SGF	0	SGP	0
			*	*	0	0	0	*	0	*
ROW Vector Mode Set	32H	1	0	0	0	0	INC			VEC
			*	*	*	*	0	0	0	0
N-line Inversion Set	34H	1	FIM	0	0	N-block Inversion				
			0	*	*	0	0	0	0	0
Driving Mode Set	36H	1	0	0	SPT	0	SCS	CC	CCM	LFS
			*	*	0	0	0	0	0	0
Entry Mode Set	40H	1	16B	0	0	MDI	0	0	Y/X	RMW
			0	*	*	0	*	*	0	0
Row address Area Set	42H	2	Y Start address set							
			0	0	0	0	0	0	0	0
			Y end address set							
			1	0	0	0	0	0	1	1
Column ddress Area Set	43H	2	X start address set							
			0	0	0	0	0	0	0	0
			X end address set							
			1	0	0	0	0	0	1	1
RAM Skip Area Set	45H	1	0	0	0	0	0	0	RSK	
			*	*	*	*	*	*	0	0
Specified Display Pattern Set	53H	1	0	0	0	0	0	0	SDP	
			*	*	*	*	*	*	0	0
Partial Display Mode Set	55H	1	0	0	0	0	0	PDTY	PDM	PT
			*	*	*	*	*	0	0	0
Partial Display Start Line Set	56H	1	Partial start line							
			0	0	0	0	0	0	0	0
Partial Display End Line Set	57H	1	Partial end line							
			0	0	0	0	0	0	0	0

Table 23.Instruction Parameter (Continued)

Instruction	Hex	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Area Scroll Mode Set	59H	4	0	0	0	0	0	0	SCM	
			*	*	*	*	*	*	0	0
			Scroll area start line							
			0	0	0	0	0	0	0	0
			Scroll area end line							
			1	0	0	0	0	0	1	1
			Lower Fixed number							
			0	0	0	0	0	0	0	0
Scroll Start Line Set	5AH	1	Scroll start line							
			0	0	0	0	0	0	0	0
Offset Volume Set	EDH	1	1	1	1	0	1	1	0	1
			*	*	P5	P4	P3	P2	P1	P0

*: Don't care
Parameter: The number of parameter bytes that follows instruction data.

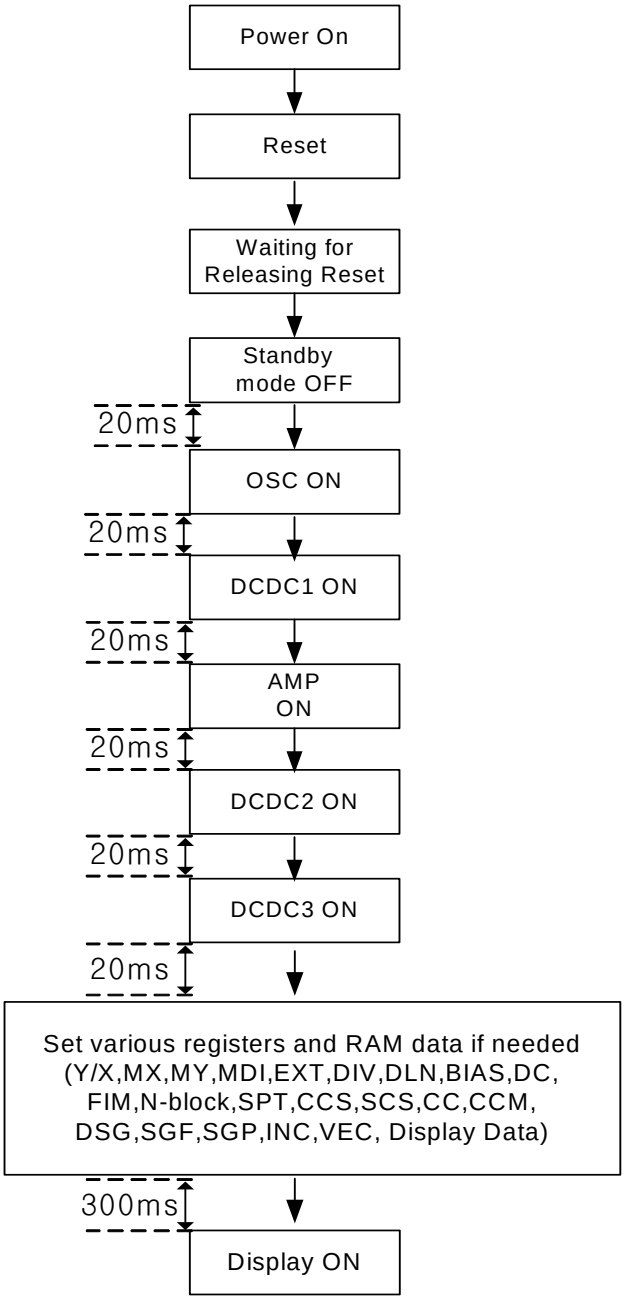
Reset Operation

When RSTB becomes “L”, following procedure is occurred.

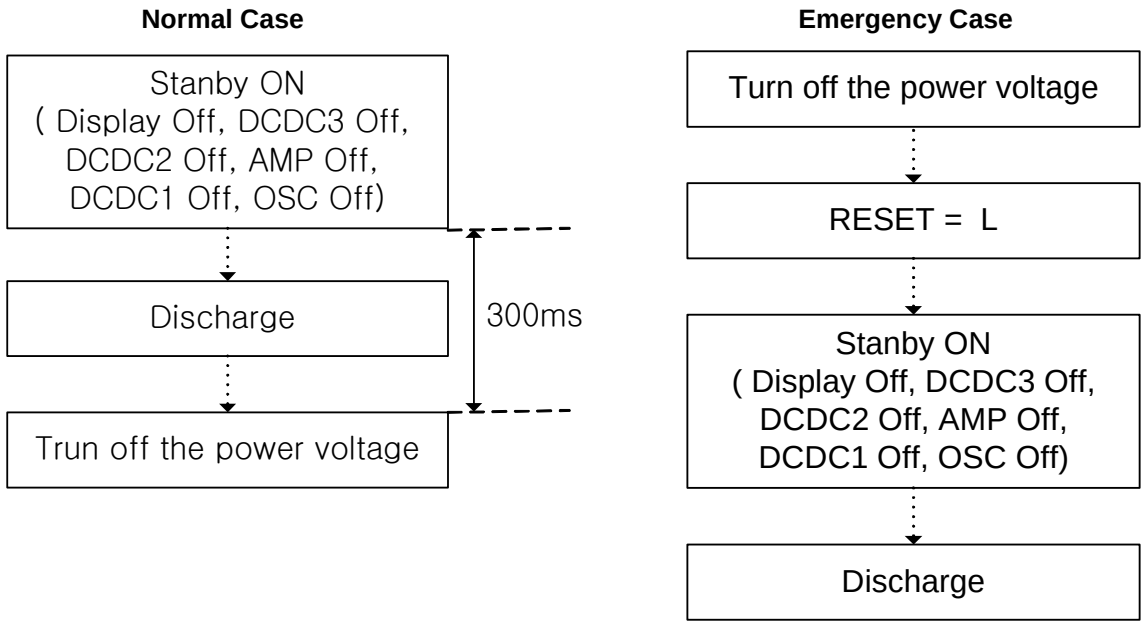
- X start address: 0, X end address: 131
- Y start address: 0, Y end address: 131
- Display OFF
- Read Modify Write Mode OFF
- Function Mode Set
  OSC = 0: Oscillator OFF
  EXT = 0: Internal Oscillator Mode
  16B = 0: Data Bus Width 16bit Mode
  MDI = 0: Memory Data Inversion OFF
  MX = 0: Column Address increment
  MY = 0: Row Address increment
  Y/X = 0: X-address Count Mode
  Standby Mode ON
- Driving Mode Set
  SPT = 0: Equally Distributed MLA
  SCS = 0: Segment charge share mode OFF
  CC = 0: Crosstalk compensation mode OFF
  CCM = 0: The coefficient of crosstalk compensation is 1/4
- DCDC Clock Division Set
  DIV = 0000
- Duty Set
  Display Duty : DLN = 00 (132 duty)
- DC-DC Select : DC = 0: X1 step-up
- Bias Set
  Bias = 00: 1/4 bias
- DC/DC and AMP ON/OFF Set
  AMP = 0: Built-in OP-AMP OFF
  DCDC1 = 0: Built-in 1’st booster OFF
  DCDC2 = 0: Built-in 2’nd booster OFF
  DCDC3 = 0: Built-in 3’rd booster OFF
- N-block inversion
  FIM = 0: Forcing Inversion OFF
  N-block inversion = 0DH: frame inversion
- Partial Display Mode
  PT = 0: Partial Display Mode OFF
- Partial Display Area Set
  Partial start line = 00H
  Partial end line = 00H
-Area Scroll Set
  Mode = 00H : Entire Display Scroll Mode
  Area Start Line: 00H
  Area End Line: 83H
  Lower Fixed Line Number: 00H
- Scroll Start Line Set
  Scroll Start Line: 00H
- Addressing Mode Set
  DSG = 0: Mode 0
  SGF = 0: SG Frame Inversion OFF
  SGP = 0: Same phase in all pixel
- Row Vector Mode Set
  INC =111: Increment every subframe
  VEC=0: R1->R2->R3->R4->R1->…

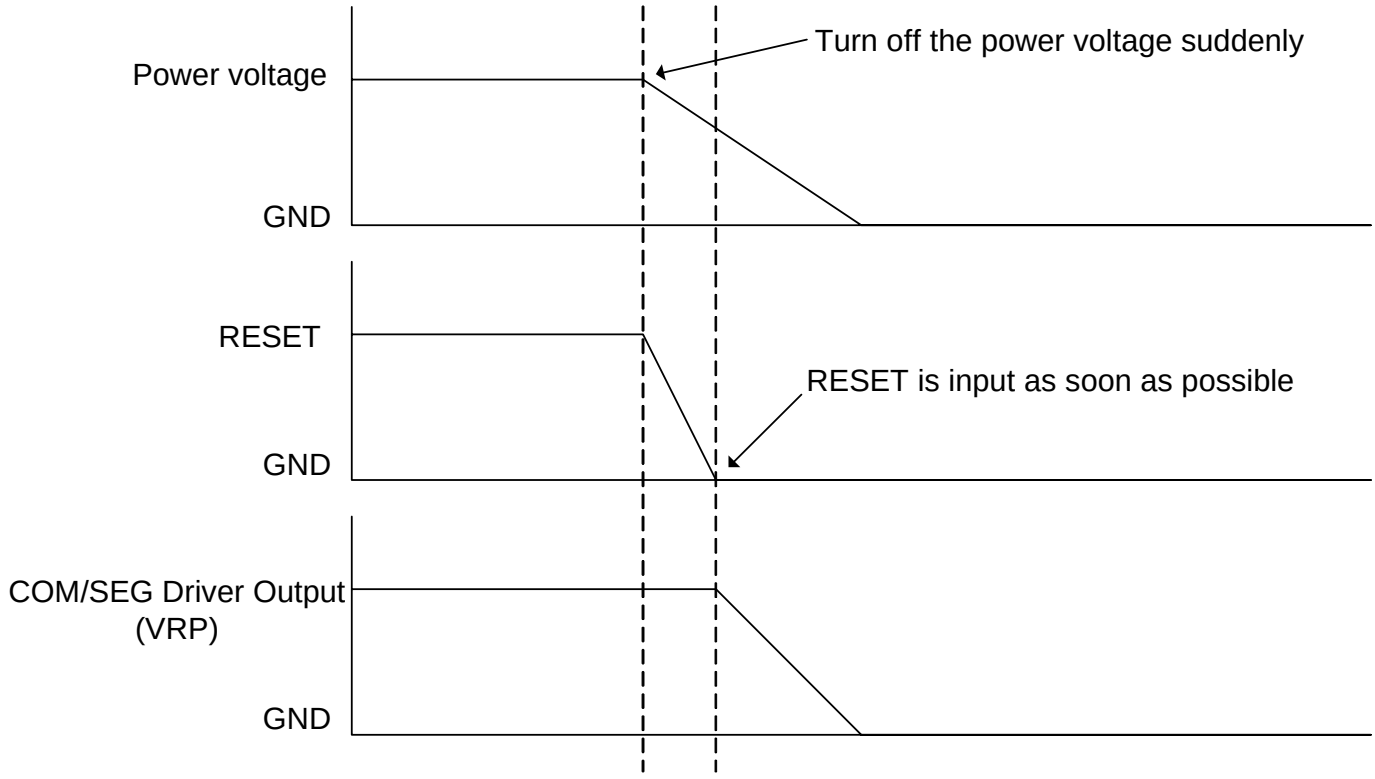
POWER ON/OFF SEQENCE

Power ON Sequence



Power OFF Sequence



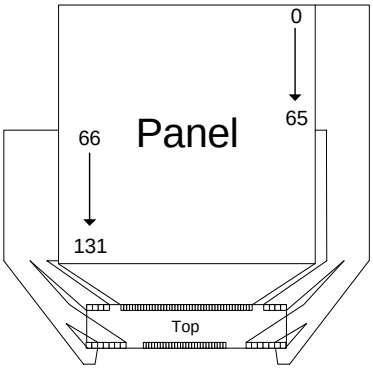


Note: When the signal of the hardware reset comes during the power-off period, COM/SEG output is forcibly lowered to the GND levels. Discharge resistor must be added at VCC pin. Refer application system diagram (page 78)

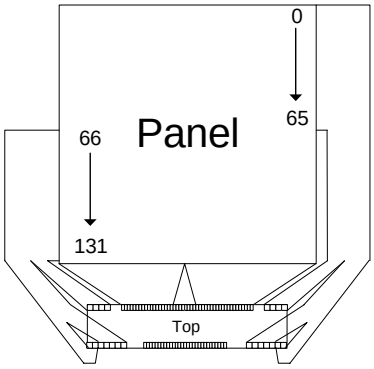
DISPLAY APPLICATIONS BETWEEN S6B33B3 AND PANEL

By combination of DLN, CDIR, RSK bits setting, LCD panel and S6B33B3 can be connected in many ways.

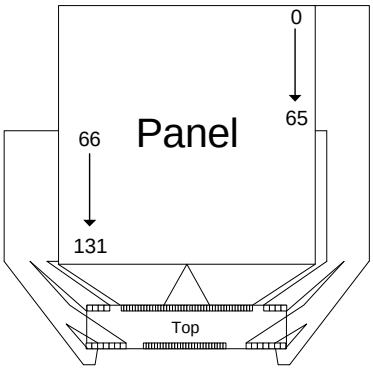
1) 132 DUTY DISPLAY



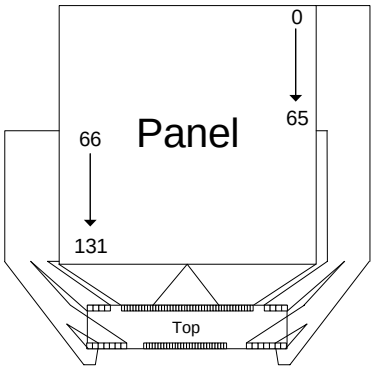
DLN = 00
CDIR = 0
RSK = 00
(132RGB)



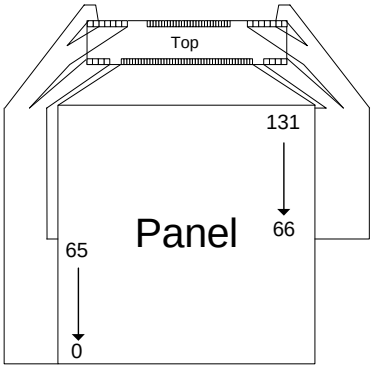
DLN = 00
CDIR = 0
RSK = 10
(120RGB)



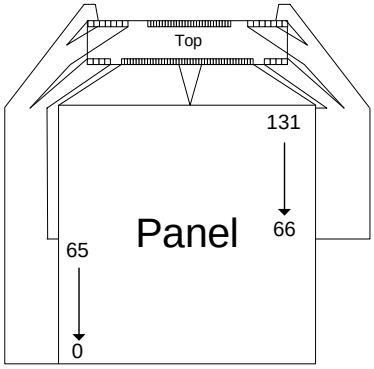
DLN = 00
CDIR = 0
RSK = 01
(104RGB)



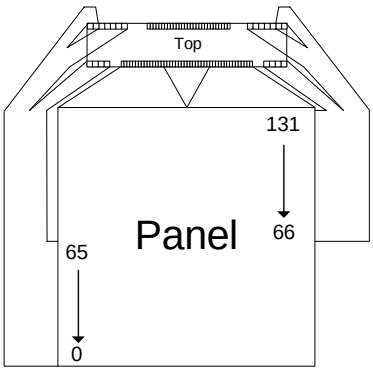
DLN = 00
CDIR = 0
RSK = 11
(96RGB)



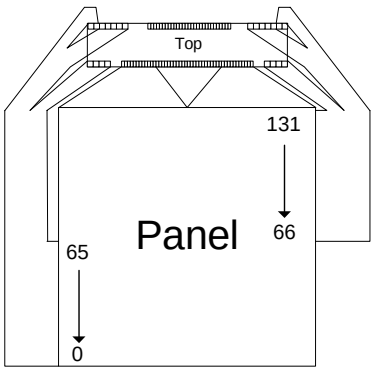
DLN = 00
CDIR = 1
RSK = 00
(132RGB)



DLN = 00
CDIR = 1
RSK = 10
(120RGB)

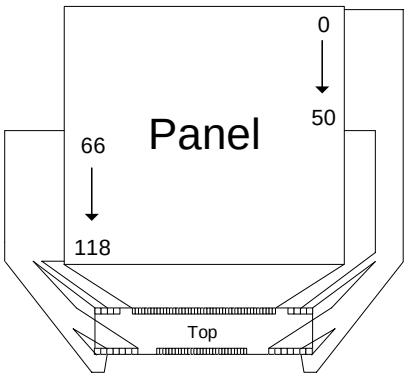


DLN = 00
CDIR = 1
RSK = 01
(104RGB)

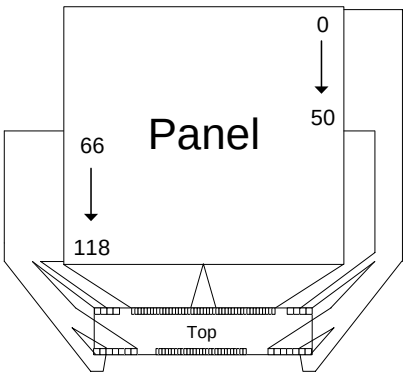


DLN = 00
CDIR = 1
RSK = 11
(96RGB)

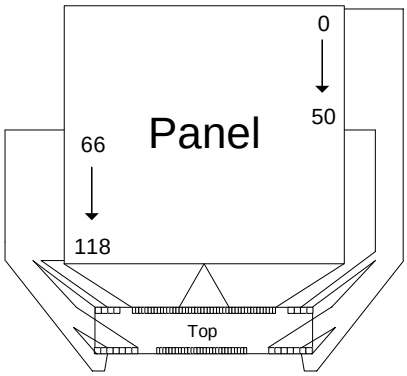
2) 104 DUTY DISPLAY



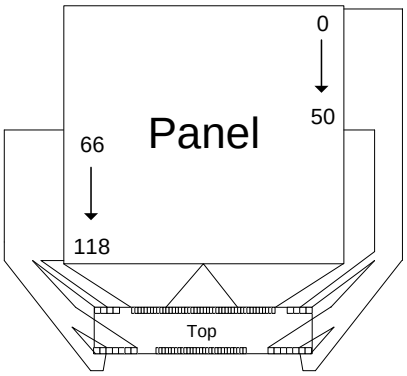
DLN = 01
CDIR = 0
RSK = 00
(132RGB)



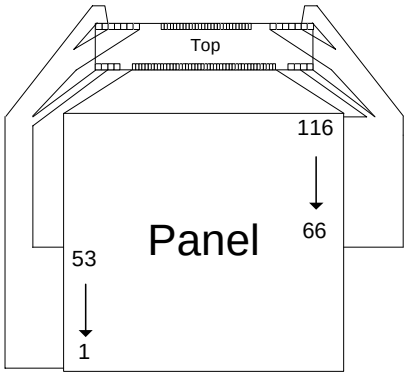
DLN = 01
CDIR = 0
RSK = 10
(120RGB)



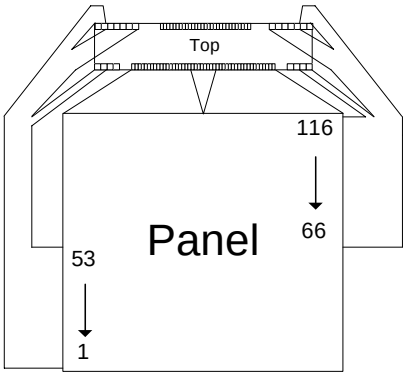
DLN = 01
CDIR = 0
RSK = 01
(104RGB)



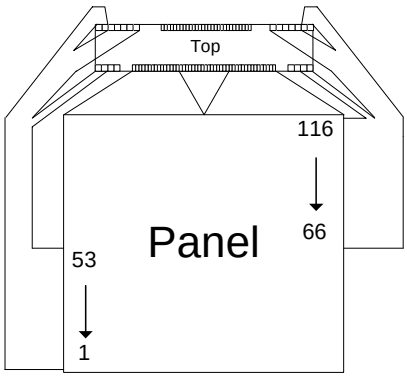
DLN = 01
CDIR = 0
RSK = 11
(96RGB)



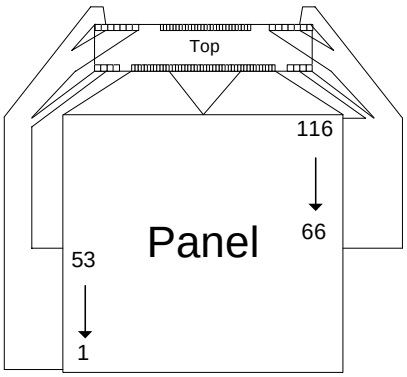
DLN = 01
CDIR = 1
RSK = 00
(132RGB)



DLN = 01
CDIR = 1
RSK = 10
(120RGB)

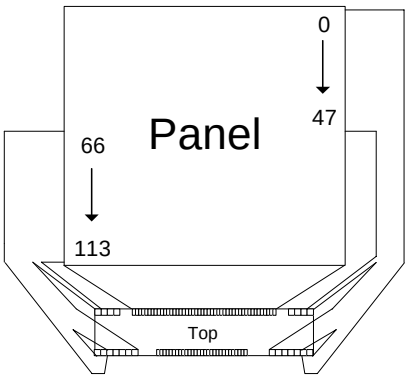


DLN = 01
CDIR = 1
RSK = 01
(104RGB)

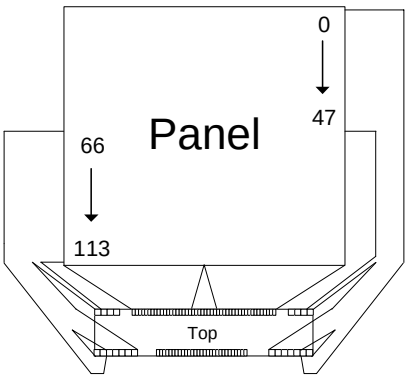


DLN = 01
CDIR = 1
RSK = 11
(96RGB)

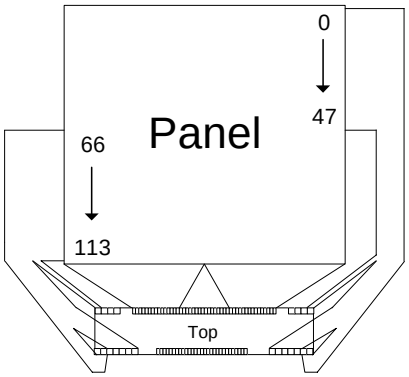
3) 96 DUTY DISPLAY



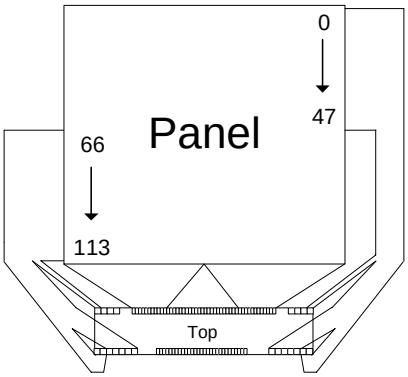
DLN = 11
CDIR = 0
RSK = 00
(132RGB)



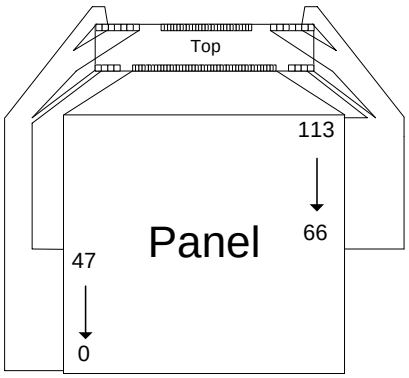
DLN = 11
CDIR = 0
RSK = 01
(120RGB)



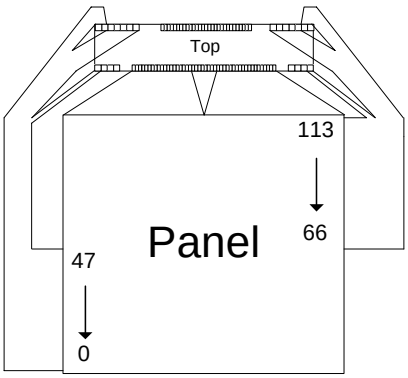
DLN = 11
CDIR = 0
RSK = 01
(104RGB)



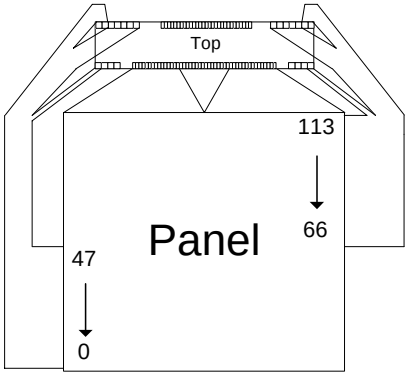
DLN = 11
CDIR = 0
RSK = 11
(96RGB)



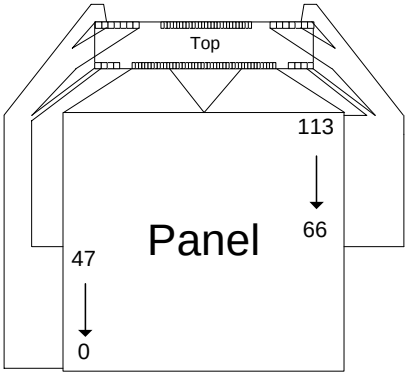
DLN = 11
CDIR = 1
RSK = 00
(132RGB)



DLN = 11
CDIR = 1
RSK = 10
(120RGB)

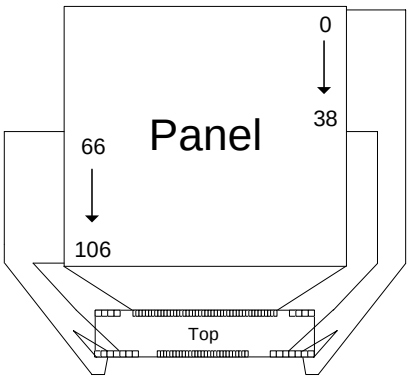


DLN = 11
CDIR = 1
RSK = 01
(104RGB)

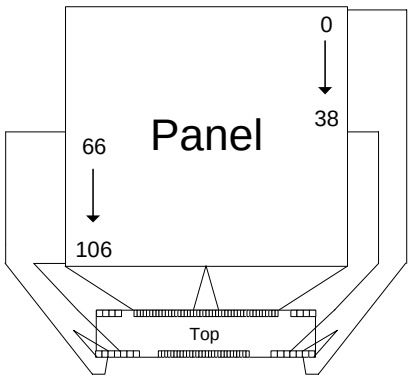


DLN = 11
CDIR = 1
RSK = 11
(96RGB)

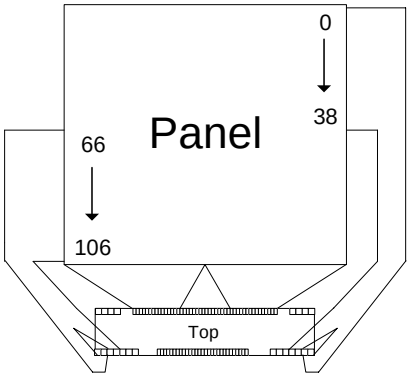
4) 80 DUTY DISPLAY



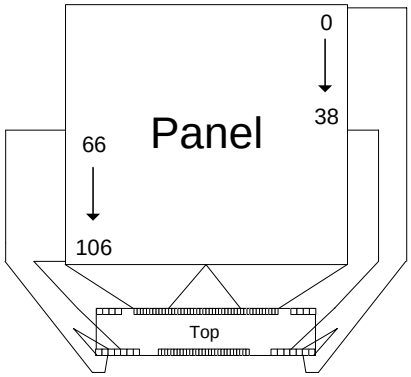
DLN = 10
CDIR = 0
RSK = 00
(132RGB)



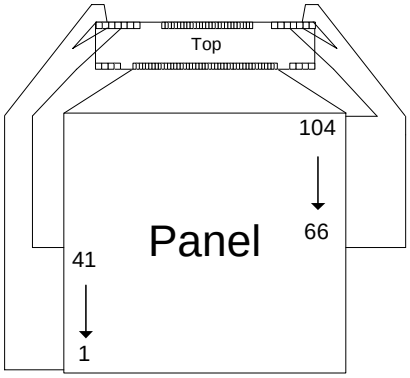
DLN = 10
CDIR = 0
RSK = 10
(120RGB)



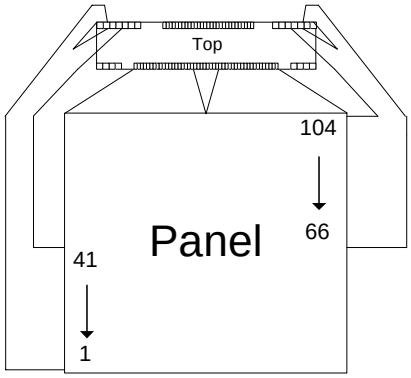
DLN = 10
CDIR = 0
RSK = 01
(104RGB)



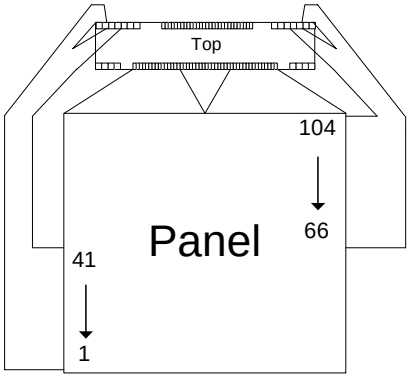
DLN = 10
CDIR = 0
RSK = 11
(96RGB)



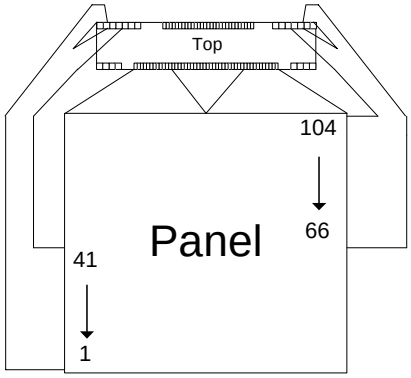
DLN = 10
CDIR = 1
RSK = 00
(132RGB)



DLN = 10
CDIR = 1
RSK = 10
(120RGB)



DLN = 10
CDIR = 1
RSK = 01
(104RGB)



DLN = 10
CDIR = 1
RSK = 11
(96RGB)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage range	VDD3	-0.3 to +4.0	V
	VDD	-0.3 to +2.15	
	VIN1	-0.3 to +4.0	
LCD Supply Voltage range	|VCC – VEE|	24	V
Input Voltage range	Vin	- 0.3 to VDD3 +0.3	V
Operating Temperature range	TOPR	-30 to +70	°C
Storage Temperature range	TSTR	-55 to +150	°C

OPERATING VOLTAGE

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (1)	VDD3	1.8	-	3.3	V
Supply Voltage (2)	VDD	1.8 ± 0.15			V
Supply Voltage (3)	VIN1 (*1)	2.4	3.0	3.3	V
Supply Voltage (4)	VIN2	2.4	3.0	4.95	V

(*1) VIN1 = VIN1R, VIN1A

DC CHARACTERISTICS (1)

(Vss = 0V, V_{DD3} = 1.8 to 3.3V, Ta = -30 to 70 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Operating voltage		VDD3		1.8		3.3	V	VDD3
Operating voltage		VIN1		2.4	-	3.3	V	VCI
Operating voltage		DC2IN	1/4 bias(x-3)	1.5	-	3.0	V	DC2IN
			1/5 bias(x-3)	2.0	-	4.0	V	
			1/5 bias(x-4)	1.33	-	2.67	V	
			1/6bias(x-4)	1.67		3.33	V	
Operating voltage		VIN2		2.4	-	4.95	V	VIN2
Operating voltage		VIN45		2.4	-	4.95	V	VIN45
Operating voltage		2Vr	2Vr = |(+VR)- (-VR)|	4.0	-	20	V	+VR, -VR
Output voltage		VREG	REG OUT voltage	1.8 ± 0.15			V	VREG
Driving voltage input range		VM	External power supply mode	1.0		2.0	V	VM
		VCC		5.0		12.0	V	VCC
		VEE		-8.0		-3.0	V	VEE
Input voltage	High	V_{IH}		0.8VDD	-	VDD	V	
	Low	V_{IL}		VSS	-	0.2VDD		
Output voltage	High	V_{OH}	I_{OH} = 0.5mA	0.8VDD	-	VDD	V	
	Low	V_{OL}	I_{OL} = 0.5mA	VSS	-	0.2VDD		
Input leakage current		I_{IL}	VIN = VDD or VSS	-1.0	-	+1.0	µA	
Output leakage current		I_{OZ}	VIN = VDD or VSS	-3.0	-	+3.0	µA	
Oscillator Frequency Tolerance	Normal or Partial 0	F_{OSC1}	(*R1)=TBD (fFR=100Hz target), DSG=0, 132 display lines	502.2	558.0	613.8	kHz	OSC1 - OSC2
	Partial 1	F_{OSC2}	(*R2)=TBD (fFR=100Hz target), DSG=0, 66 display lines	256.7	285.2	313.7	kHz	OSC3 - OSC4
Oscillator Frequency Range	Normal or Partial 0	F_{OSC1}	(*1)	227.7		763.8	kHz	OSC1 - OSC2
	Partial 1	F_{OSC2}	(*2)	95.5		381.9	kHz	OSC3 - OSC4
Driving voltage input range		V1 VM		2.0 1.0	-	4.0 2.0	V	

Note : (*R1),(*R2) resistances are only recommended to get target frame frequency. But the value is not absolute.

(*1) Minimum oscillator frequency range is defined at fFR=70Hz and display line number=96
Maximum oscillator frequency range is defined at fFR=140Hz and display line number=132
(*2) Minimum oscillator frequency range is defined at fFR=70Hz and display line number=36
Maximum oscillator frequency range is defined at fFR=140Hz and display line number=66

DC CHARACTERISTICS (2)

(Vss = 0V, V_{DD3} = 1.8 to 3.3V, VIN1=2.4 to 3.3V, Ta = -30 to 70 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Driver output resistance	SEG	R_{ON-Seg}	V1=3.3 V, VM=1.65V, V0=0V, Ta = 25°C, Iload=100uA	-	1.5	3.0	kΩ	SEGn
	COM	R_{ON-Com}	VCC=12 V, VM=1.5V, VEE=-9.0V, Ta = 25°C, Iload=100uA	-	1.5	2.0	kΩ	COMn
Current consumption	Normal Mode	IDD	VDD3=VIN1=3.0V, V1=3.0V, Bias(1)=1/6, DC(1)=x1.5, Ta=25°C, Display line=132 DSG=0 (1dummy) f_{OSC}=545.6kHz (fFR=100Hz) No load, No access, All white pattern	-	TBD	TBD	μA	VDD3+ VIN1

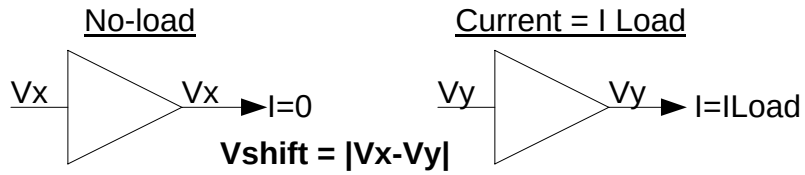
* : “TBD” is determined from lowest power consumption for dc-dc converter.

DC CHARACTERISTICS (3)

(Vss = 0V, V_{DD3} = 1.8 to 3.3V, VIN1=2.4 to 3.3V, Ta = -30 to 70 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Voltage shift range(*1)	Δ (+VR)	Isource = 80uA	-	-	150	mV	+VR
	Δ (V1)	Isource = 250uA	-	-	20	mV	V1
	Δ (VM)	Isource,sink = 250uA	-	-	40	mV	VM
	Δ (-VR)	Isink = 80uA	-	-	150	mV	-VR

(*1) Voltage shift means output voltage difference between output current = Iload and no-load.
Refer to the following figure. (in case of source current mode)



Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Tolerance of Bias ratio	Δ (+VR)_0 Δ (-VR)_0(*1)	No load	-200	-	+200	mV	+VR -VR

(*1) Tolerance of bias ratio definition
Δ (+VR)_0 = ((+VR) - VM) – VM *Bias
Δ (-VR)_0 = (VM - (-VR)) – VM *Bias

DC CHARACTERISTICS (4)

(Vss = 0V, V_{DD3} = 1.8 to 3.3V, VIN1=2.4 to 3.3V, Ta = -30 to 70 °C)

Item	Symbol	Condition		Min	Typ	Max	Unit	Remarks
Temperature compensation	ΔVt	VDD=VIN1=V1=3.0V, -20 to 70 °C		-0.02	-	+0.02	%/°C	V1
Tolerance of Contrast step of V1	ΔVstep	V1 = 4V		3.92	7.84	11.76	mV	V1
Voltage range	ΔV1 ΔVM	Contrast set = FFh	V1	3.95	4.0	4.05	V	V1
			VM	1.95	2.00	2.05	V	VM
		Contrast set = 00h	V1	1.95	2.00	2.05	V	V1
			VM	0.95	1.00	1.05	V	VM

Item			Condition		Max	Unit	Ref
			Load current	Voltage range			
Offset Voltage	‖+VR-VM‖ -‖VM -(-VR)‖		I Load = +100uA (+VR) I Load = -100uA (-VR)	+VR=5.0~TBD V V1=2.0~4.0V VM=1.0~2.0V -VR=-3.0~-TBD V	100	mV	Fig.1
	‖V1-VM‖ -‖VM-V0‖	A	I Load = +100uA (V1, VM)		50	mV	Fig.2
		B	I Load = +100uA (+VR) I Load = -100uA (-VR)				

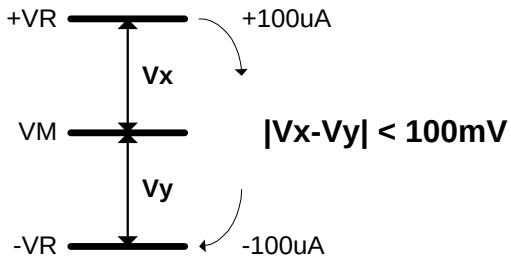


Fig. 1: Offset voltage definition (+VR,VM,-VR)

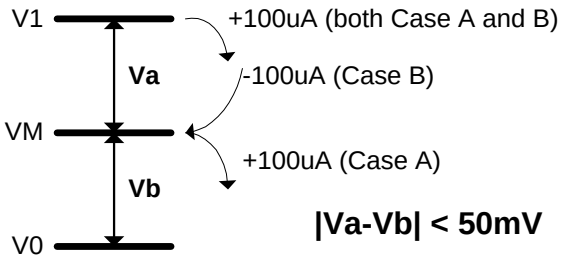


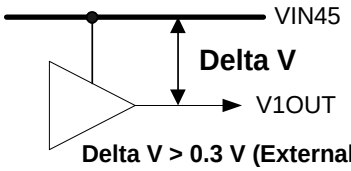
Fig. 2: Offset voltage definition (V1,VM,V0)

DC CHARACTERISTICS (5)

(Vss = 0V, V_{DD3} = 1.8 to 3.3V, VIN1=2.4 to 3.3V, Ta = -30 to 70 °C)

Item		Range	
		Min	Max (DC(1) and DC(2) = X1.5)
Voltage Level	V1OUT	2.0 V	4.0 V(*1)
	VMOUT	1.0 V	2.0 V(*2)
	DC2OUT	1.33 V (1/5 Bias)	2.75 V(*3) (1/6 Bias)

(*1) This definition is shown as below



Delta V > 0.3 V (External VIN45)

Delta V > 0.5 V (VIN45 = VOUT45)

If V1OUT input voltage is set over VIN45, V1OUT output voltage must be clipped near VIN45. In this case, V1OUT output level must not be unstable. Refer to Fig.1

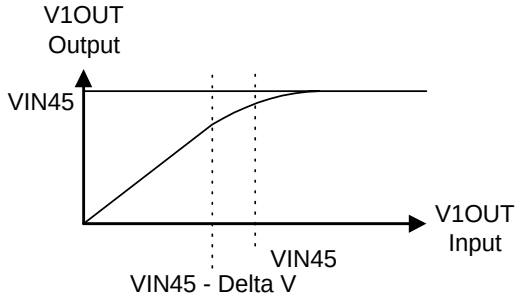
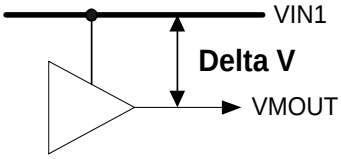


Fig. 1

(*2) This definition is shown as below



Delta V > 0.3 V

If VMOUT input voltage is set over VIN1, VMOUT output voltage must be clipped near VIN1.
In this case, VMOUT output level must not be unstable. Refer to Fig.2

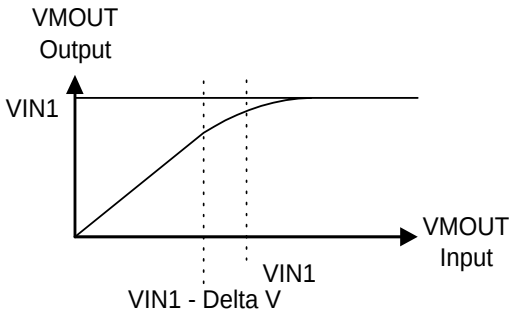
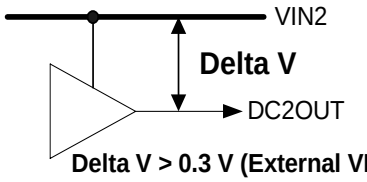


Fig. 2

(*3) This definition is shown as below



Delta V > 0.3 V (External VIN2)

Delta V > 0.5 V (VIN2 = VOUT45)

If DC2OUT input voltage is set over VIN2, DC2OUT output voltage must be clipped near VIN2. In this case, DC2OUT output level must not be unstable. Refer to Fig.3

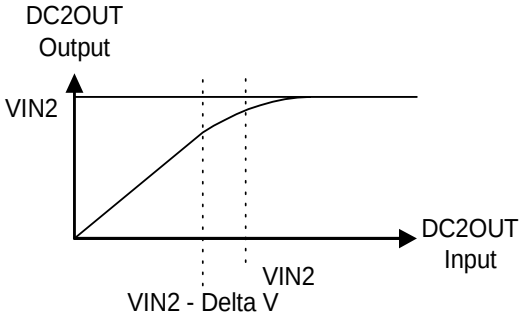
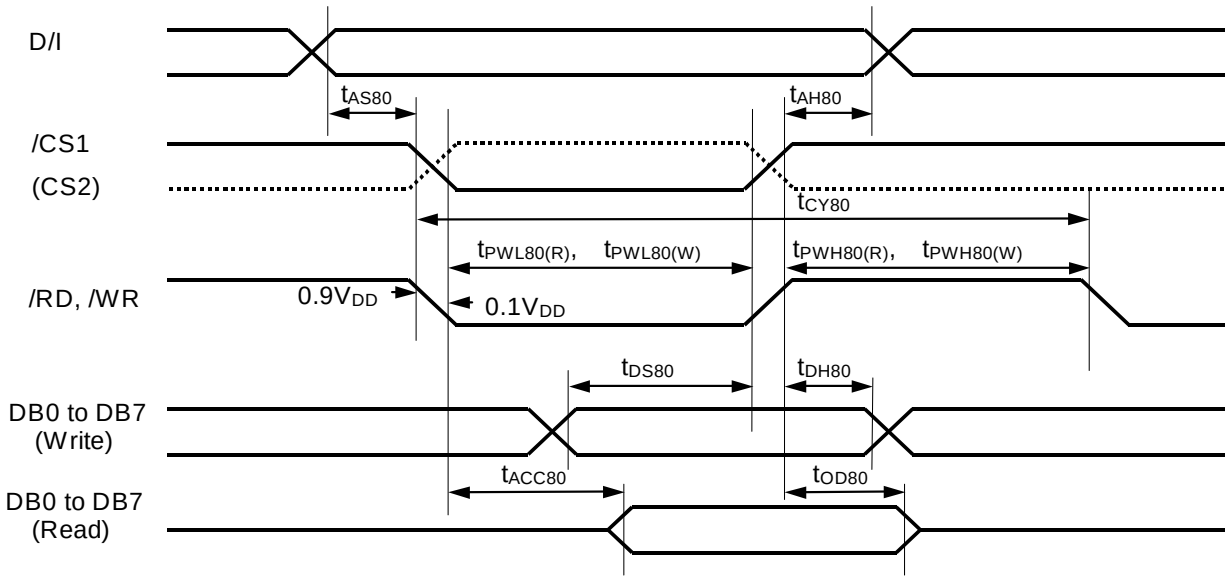


Fig.3

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)



** $t_{PWL80(W)}$ and $t_{PWL80(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and /WR(/RD) is low.

Figure 24.Parallel Interface (8080-series MPU) Timing Diagram

Table 24.AC Characteristics (8080-series Parallel Mode)

(VDD = 1.8 Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Typical	Unit
Address setup time Address hold time	D/I	t_{AS80} t_{AH80}		TBD TBD	ns
System cycle time		t_{CY80}		TBD	ns
Pulse width low for write Pulse width High for write	WRB (WRB)	$t_{PWL80(W)}$ $t_{PWH80(W)}$		TBD TBD	ns
Pulse width low for read Pulse width high for read	RDB (RDB)	$t_{PWL80(R)}$ $t_{PWH80(R)}$		TBD TBD	ns
Data setup time Data hold time	DB0 to DB15	t_{DS80} t_{DH80}		TBD TBD	ns
Read access time Output disable time		t_{ACC80} t_{OD80}	CL = 100 pF	TBD	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.
(tr + tf) < (t_{CY80} – $t_{PWL80(W)}$ – $t_{PWH80(W)}$) for write, (tr + tf) < (t_{CY80} – t_{PWLR80} – t_{PWHR80}) for read

Read / Write Characteristics (6800-series Microprocessor)

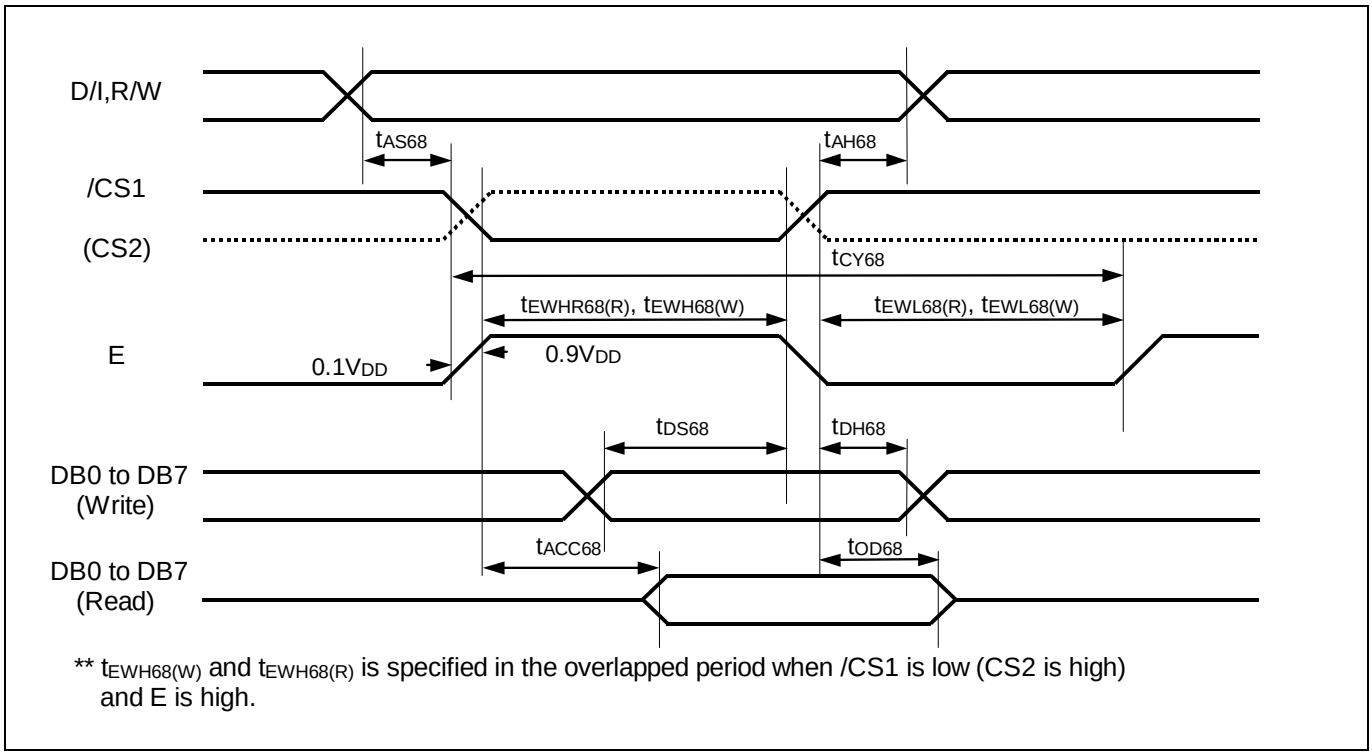


Figure 25.Parallel Interface (6800-series MPU) Timing Diagram

Table 25.AC Characteristics (6800-series Parallel Mode)

(V_{DD3} = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Typical	Unit
Address setup time Address hold time	D/I R/W	t_{AS68} t_{AH68}		TBD TBD	ns
System cycle time		t_{CY68}		TBD	ns
Enable width high for write Enable width low for write	RDB (E)	$t_{EWH68(W)}$ $t_{EWL68(W)}$		TBD TBD	ns
Enable width high for read Enable width low for read	RDB (E)	$t_{EWH68(R)}$ $t_{EWL68(R)}$		TBD TBD	ns
Data setup time Data hold time	DB0 to DB15	t_{DS68} t_{DH68}		TBD TBD	ns
Read access time Output disable time		T_{ACC68} t_{OD68}	C_L = 100 pF	TBD	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.
(tr + tf) < (t_{CY68} – $t_{EWH68(W)}$ – $t_{EWL68(W)}$) for write, (tr + tf) < (t_{CY68} – $t_{EWH68(R)}$ – $t_{EWL68(R)}$) for read

Serial Data Interface (4 Pin) Timing

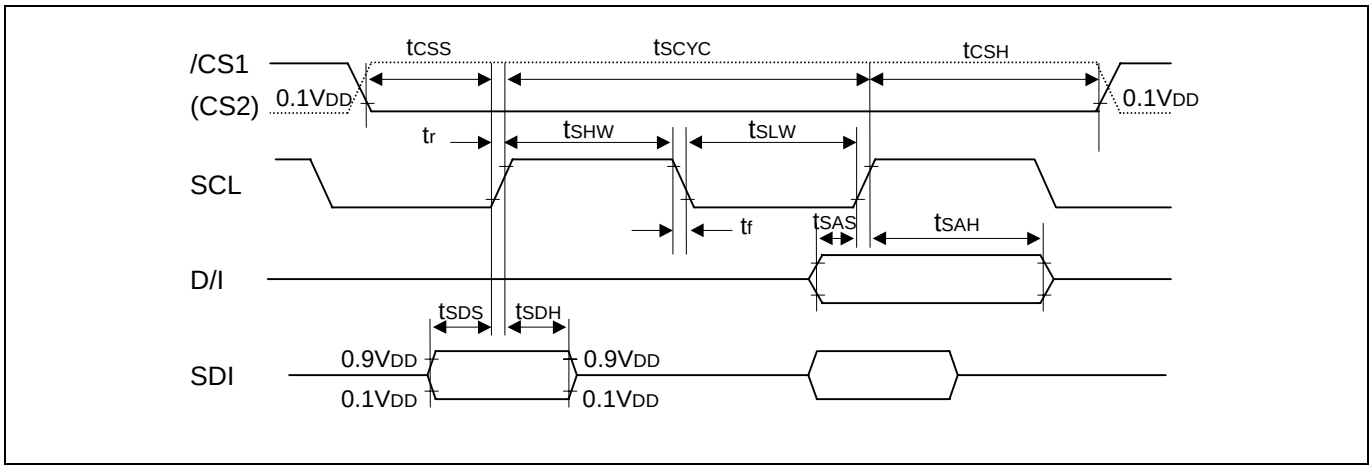


Figure 26.Serial Interface (4 Pin) Timing Diagram

Table 26.Serial Data Interface Timing

(V_{DD} = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Typical	Unit
SCL Cycle Time	SCL	t_{SCYC}		TBD	ns
SCL High Pulse Width	SCL	t_{SHW}		TBD	ns
SCL Low Pulse Width	SCL	t_{SLW}		TBD	ns
SDI Setup time	SDI	t_{SDS}		TBD	ns
SDI Hold time	SDI	t_{SDH}		TBD	ns
D/I Setup time	D/I	t_{SAS}		TBD	ns
D/I Hold time	D/I	t_{SAH}		TBD	ns
Chip Select Setup time	CS1B (CS2)	t_{CSS}		TBD	ns
Chip Select Hold time	CS1B (CS2)	t_{CSH}		TBD	ns

Serial Data Interface (3 Pin) Timing

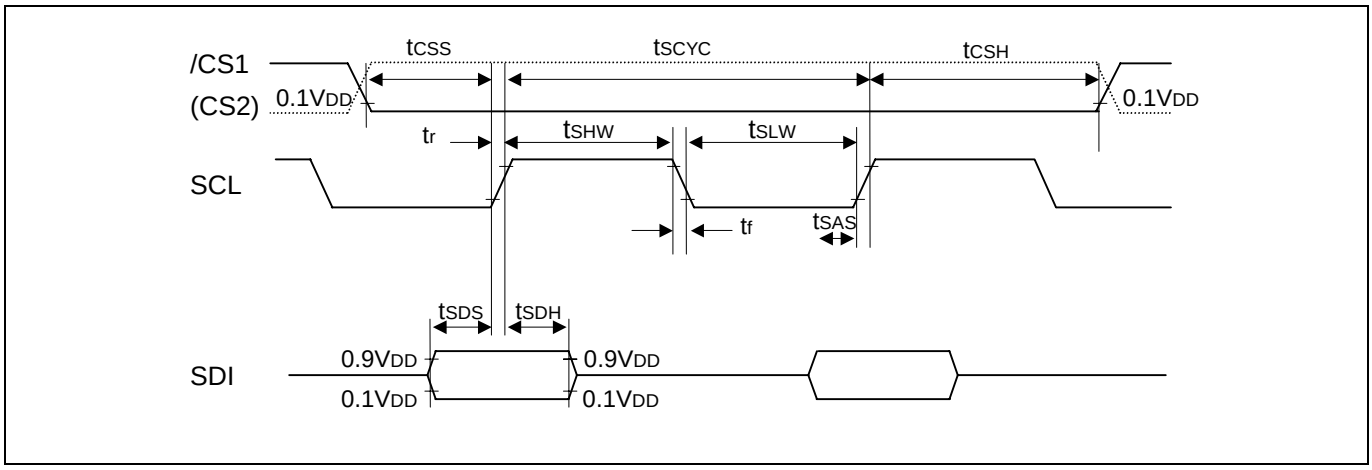


Figure 27.Serial Interface (3 Pin) Timing Diagram

Table 27.Serial Data Interface Timing

(V_{DD} = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Typical	Unit
SCL Cycle Time	SCL	t_{SCYC}		TBD	ns
SCL High Pulse Width	SCL	t_{SHW}		TBD	ns
SCL Low Pulse Width	SCL	t_{SLW}		TBD	ns
SDI Setup time	SDI	t_{SDS}		TBD	ns
SDI Hold time	SDI	t_{SDH}		TBD	ns
Chip Select Setup time	CS1B (CS2)	t_{CSS}		TBD	ns
Chip Select Hold time	CS1B (CS2)	t_{CSH}		TBD	ns

Reset Input Timing

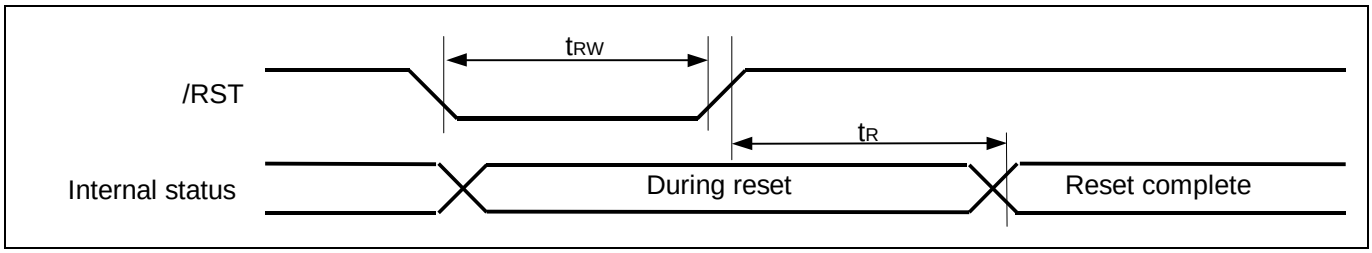


Figure 28.Reset Input Timing Diagram

Table 28.AC Characteristics (Reset mode)

(V_{DD} = 1.8 V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RSTB	T_{RW}		1000	-	ns
Reset time	-	t_R		-	1000	ns

OTP CALIBRATION MODE

SEQUENCE FOR SETTING THE MODIFIED ELECTRONIC VOLUME

- Next figure is a Block Diagram of Sequence for Setting the Modified Electronic Volume.

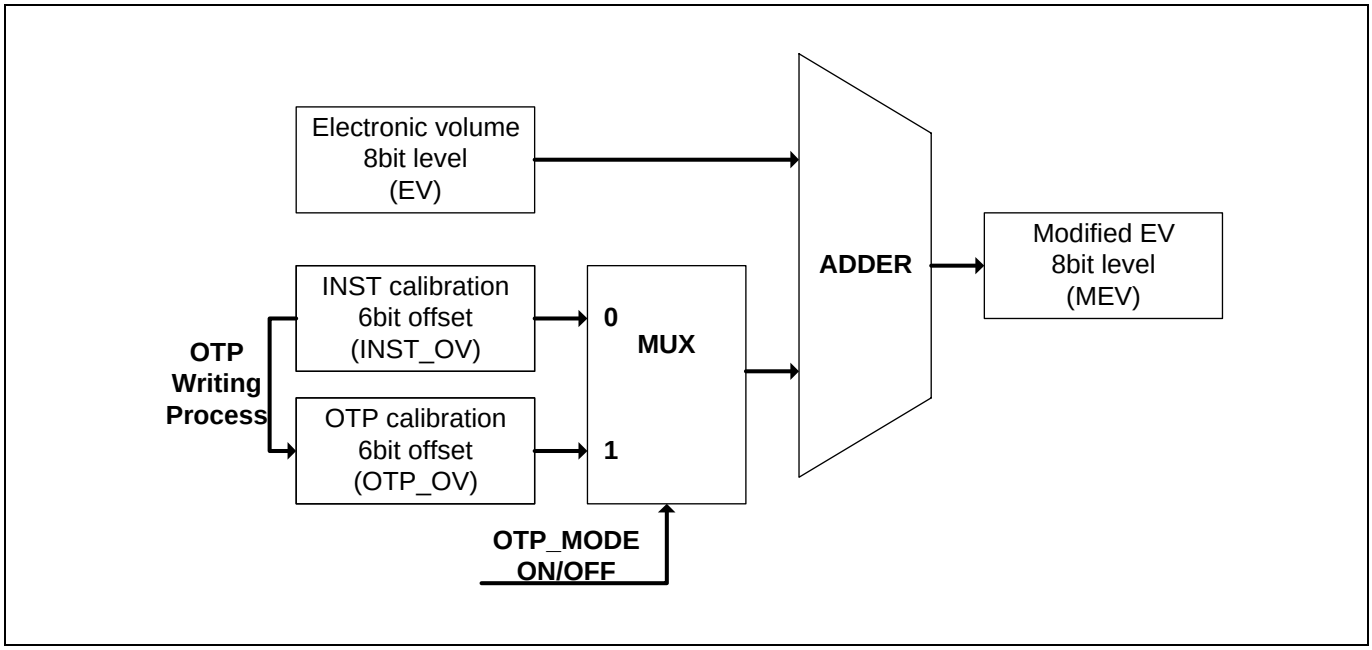


Figure 29. Sequence for Setting the Modified Electronic Volume

Initially, OTP cell is not programmed and has 6'b00000 value. When the external reset is applied, OTP mode is On. MEV is EV + OTP_OV. Since OTP_OV is 6'b00000, MEV is EV. For V1OUT calibration The instruction "OTP mode off" is executed, and then MEV is EV + OV and user can adjust MEV value using the instruction "Set offset volume register". When MEV overflows or underflows, MEV will be saturated. Repeat this step until end of the calibration. If V1OUT calibration is suitable, OTP writing process is executed, and then OTP cell is programmed and OTP_OV is programmed with OV. Finally, V1OUT calibration process is finished. Again, when the external reset is applied, OTP mode is ON. MEV is EV + OTP_OV. Accordingly MEV is the EV that has always the offset with OTP_OV value. However, if programmed OTP_OV is unlike, the instruction "OTP mode off" can be executed and then MEV will be EV + OV. Accordingly OV can be adjusted with instructions although OTP cell is programmed.

EPROM CELL STRUCTURE

OTP (One Time Programmable) has been implemented on the S6B33B3. The EPROM stores the offset volume for V1OUT calibration after the device has been assembled and calibrated on a LCD module. For OTP programming, OTPD pin and OTPG pin are used. These pins should be available to on the module glass by ITO.
The OTP block of the S6B33B3 consists of 7 bits. 1 bit is used for OTP mode protection bit (OPRT), and 6 bits are used for V1OUT calibration (OV5~OV0). OPRT can be read or written automatically in this LSI.

EPROM block

MSB LSB

OPRT	**OV5**	**OV4**	**OV3**	**OV2**	**OV1**	**OV0**

Description

OPRT : The Offset Volume(OV) can be written to EPROM cells only when OPRT bit = '0'
OV5~OV0 : The OV is used for calibrating the V1OUT voltage as an offset to the EV register value.

V1OUT CALIBRATION FLOW

V1OUT may be calibrated with OTP in the following order.(ex : EV = 32, OV=-3)

STEP	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
1.											Apply external reset (OTP data read)
2.	0	0	0	0	1	0	1	0	1	0 or 1	Set contrast control 1 or 2 by using instruction (EV = 32)
	0	0	0	0	1	0	0	0	0	0	
3.	0	0	1	1	1	0	1	0	1	0	OTP mode off by using the instruction
4.	0	0	1	1	1	0	1	1	0	1	Set offset volume by using the instruction (OV = -3)
	0	0	0	0	1	1	1	1	0	1	
5											Repeat STEP 4. Until the end of the calibration
6.											Apply programming voltages for OTP programming (OTPG=15V,OTPD=12V)
7.	0	0	0	0	1	0	1	1	0	1	Standby on by using the instruction.
8	0	0	1	1	1	0	1	1	1	1	OTP write Enable **(Only available when OPRT= 0)**
9											Apply external reset
10.											Cut off programming voltages for OTP programming (OTPG,OTPD)

After the external reset, the calibrated data are automatically transferred to the 6-bit reference voltage control register.
*Step 6, 7, 8, 9 are OTP_WRITING PROCESS.
*OTP_WRITING PROCESS is available when OPRT is zero (if OPRT = 1, OTP cell could not be programmed).

VOLTAGES AND WAVEFORMS FOR OTP PROGRAMMING

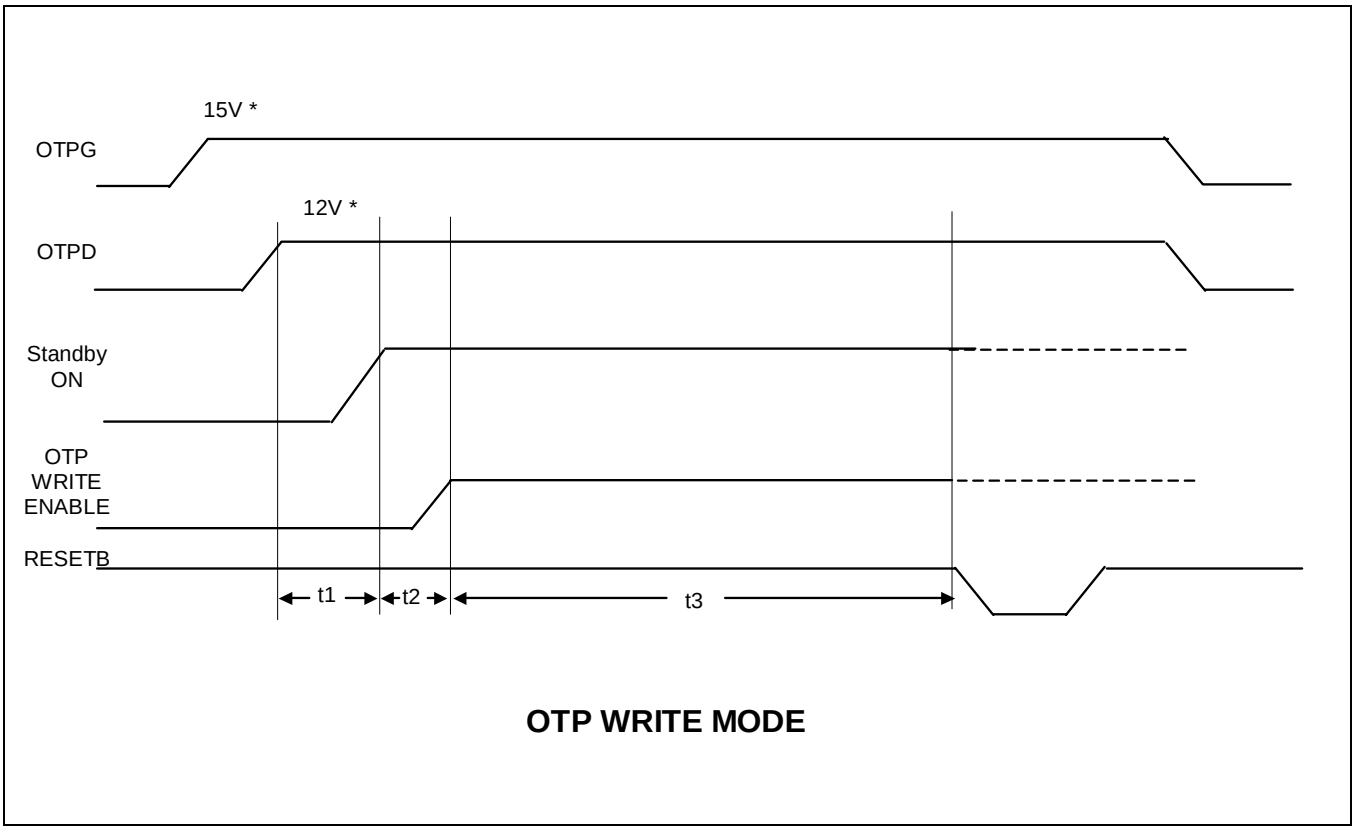


Figure 30. Voltages and waveforms for OTP programming (OTP Writing Process)

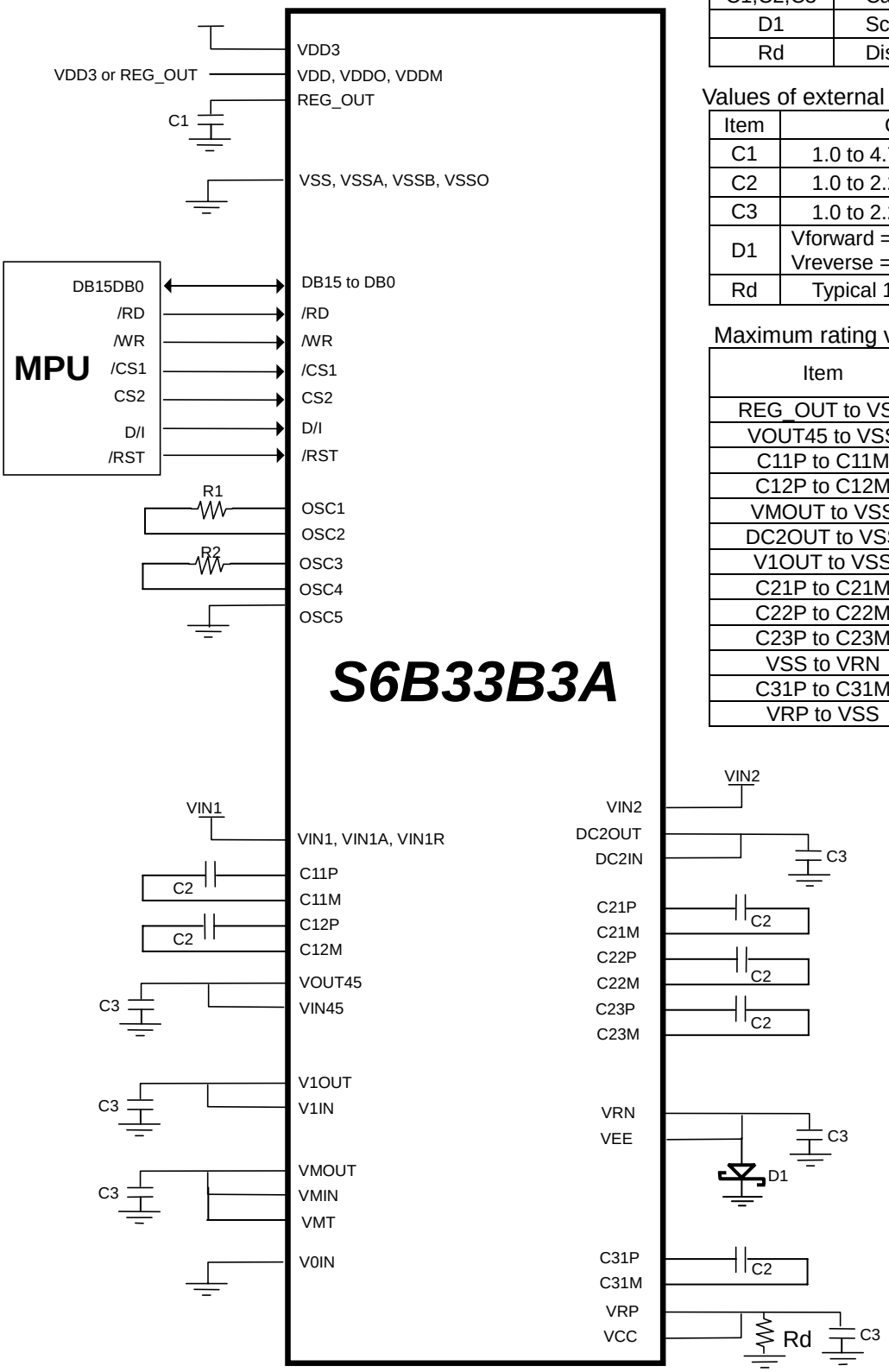
* Note : Voltages for OTPG and OTPD may be changed.

Specific timings (t1~t3)

Timing	Min	Max
t1,t2	100uS	-
t3	100mS	300mS

SYSTEM APPLICATION DIAGRAM

Internal Power Mode



External Components

Name	Device
R1,R2	Resistors
C1,C2,C3	Capacitors
D1	Schottky barrier diode
Rd	Discharge Resistor

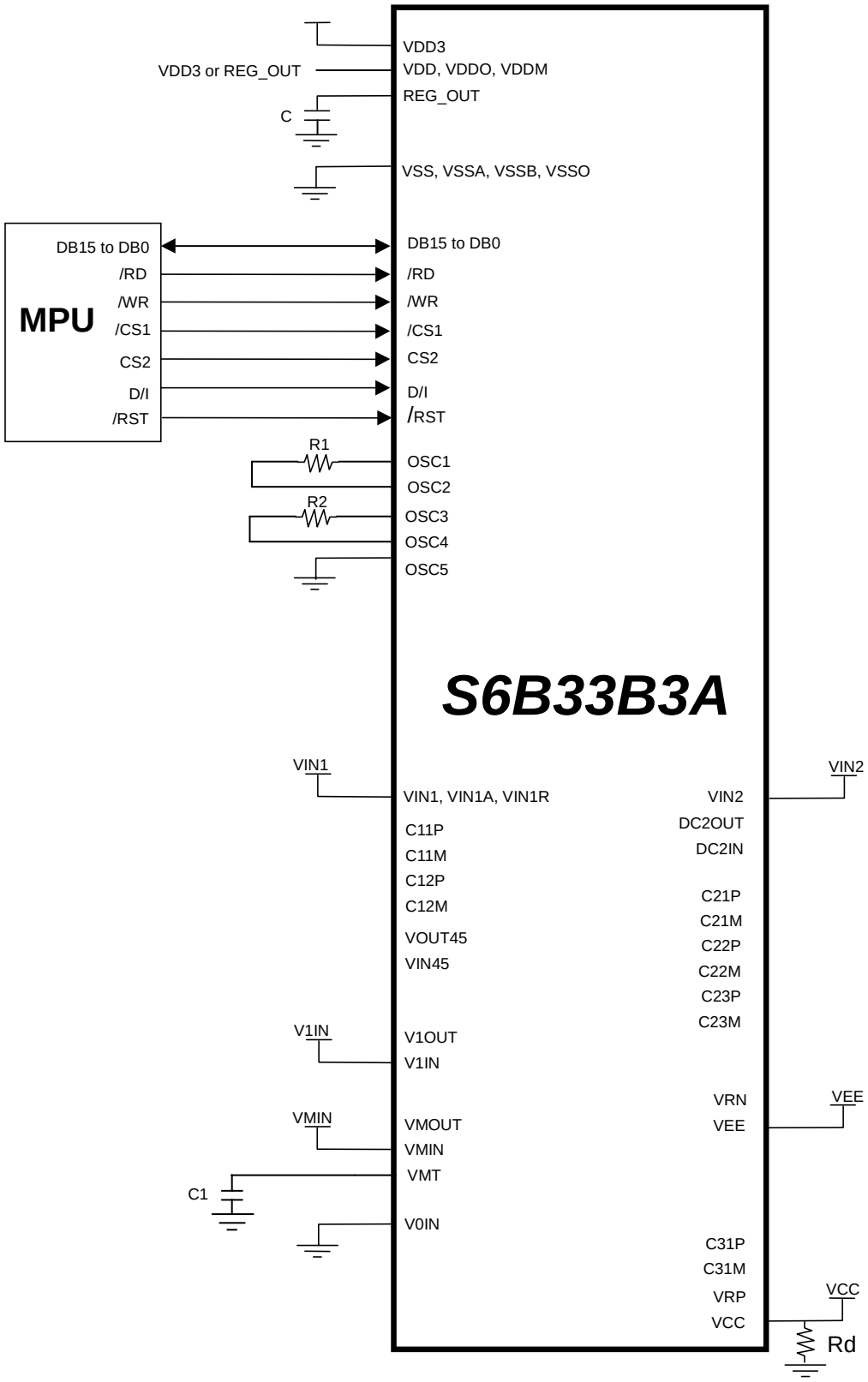
Values of external Capacitors and D1

Item	Capacitance
C1	1.0 to 4.7µF
C2	1.0 to 2.2µF
C3	1.0 to 2.2µF
D1	Vforward = Max. 0.3V at 1mA Vreverse = Min. 15V
Rd	Typical 1M ohm

Maximum rating voltage of capacitors

Item	Maximum rating voltage
REG_OUT to VSS	3V
VOUT45 to VSS	8V
C11P to C11M	6V
C12P to C12M	6V
VMOUT to VSS	3V
DC2OUT to VSS	5V
V1OUT to VSS	6V
C21P to C21M	5V
C22P to C22M	10V
C23P to C23M	13V
VSS to VRN	13V
C31P to C31M	17V
VRP to VSS	18V

External Power Mode



S6B33B3 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	May 31,2003
0.1	Preliminary Specification	September 23,2003
0.2	1. COM charge sharing scheme modified from with external capacitor to without external capacitor. 2. Insert 4,096 Gray Scale Color Mode Display 3. Insert FIR bit in Addressing Mode Set (30H) Instruction 4. Insert Discharge Resistor in SYSTEM APPLICATION DIAGRAM	October 13, 2003
0.3	1. When COM charge share is on (CCS = 1), then INC forcibly becomes subframe (INC = 111). 2. The voltage of OTPG changes from 12.5V to 15V. The voltage of OTPD changes from 10V to 12V.	November 11,2003
0.4	1. Change Instruction Set 2. Add pin coordination 3. Correct a wrong word (low → high) at Monitor Signal Control (18H) (Page 32)	November 20,2003
0.5	1. Exchange normal mode division ratio and partial mode 1 ratio at DCDC Clock Division (24H)	January 7,2004
0.6	1. Insert VDDO, VDDM in pin description (Page 11) 2. Insert VDDM in system application diagram (Page 77~78) 3. Increase output pad bump size(18umX160um →18umX170um) (Page 6) 4. Change pad center coordinates owing to bump size change. (Page 9~13)	February 4, 2004
0.7	1. Correct maximum rating of capacitors table in system application diagram. (Page 77) 2. Add the timing of power off sequence. (Page 58) 3. Correct TEST_NT pin description in Table13 Test pins (I/O:I → O). (Page 14) 4. Add VDD, VIN1 items in absolute maximum ratings. Add VDD item in operating voltage. (Page 63) 5. Correct OTP writing timing(t3) item in specific timings(Page 76)	March 2, 2004
0.8	1. Correct Table 15. (Page 15) 2. Correct Power Save ON → Standby ON in Figure 31. (Page 77)	March 8, 2004
0.9	1. Note the feature of internal oscillator.(Page 25) 2. Correct 2Vr maximum voltage 20V → 24V in DC characteristics. (Page 65)	May 27, 2004
1.0	1. The align key coordinates are changed.(Page 4) 2. Note the contrast limitation in 1/6 bias.(Page 34) 3. Remove CCS register in Driving Mode Set (Page 38) 4. Correct 2Vr maximum voltage 24V → 20V in DC characteristics. (Page 63) 5. Δ (VM) maximum voltage change from 20mV to 40mV. Δ (+VR)/ Δ (-VR) maximum voltage change from 100mV to 200mV. (Page 65)	July 1, 2004
1.1	1. Exchange the COM PAD order.(Page 5~7, Page 58~61)	August 25, 2004