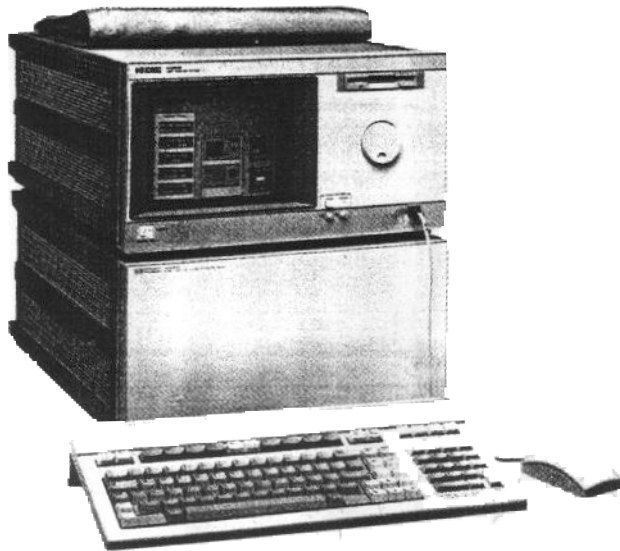
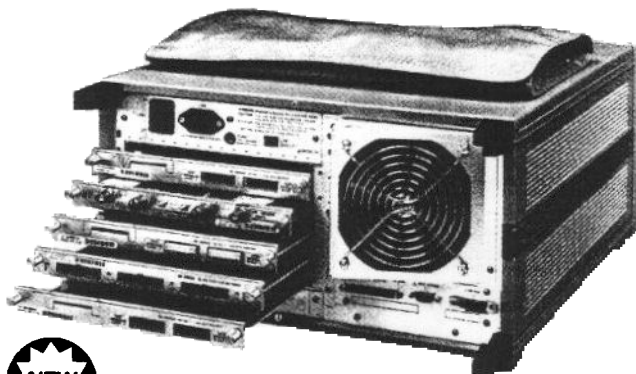


LOGIC ANALYZERS

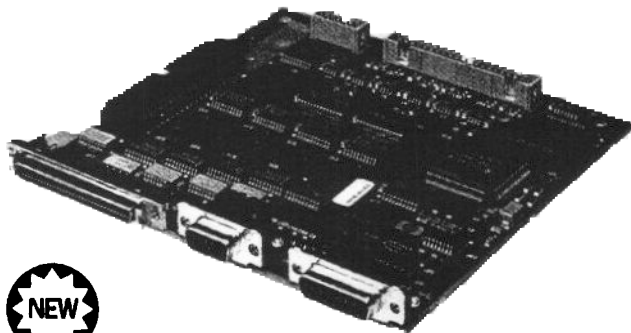
Logic Analysis System
HP 16500B and Measurement Modules



The HP 16500B's touchscreen, keyboard, or mouse driven interface delivers superior ease-of-use.



The HP 16500B and HP 16501A support up to ten simultaneous measurement modules.



The HP 16500L interface card provides an Ethernet port as well as a connector for the HP 16501A expansion frame.

- Modular, configurable logic analysis system
- Expandable, up to ten different modules
- Powerful cross-module triggering
- Extensive microprocessor support
- Connectivity to your computer

HP 16500B Modular Logic Analysis System

The HP 16500B Logic Analysis System can be configured for a wide range of measurement tasks, including microprocessor debug, hardware design verification and debug, software performance analysis, characterization, and functional pass/fail testing. Start with a focused system, then expand as your needs evolve. The HP 16500B accepts up to five different measurement modules.

HP 16501A Expansion Frame

The expansion frame provides an additional five slots to your HP 16500B, giving you control of up to ten measurement modules. You can now cross-trigger up to ten measurement modules and then view your results on the same screen with 2 ns time correlation.

HP 16500L Logic Analysis Interface Card

This optional card includes an Ethernet port, video out port, and a connector for the HP 16501A expansion frame. The HP 16500L interface card lets you mount the HP 16500B to your computer so you can network your measurement data and screen images using the Network File System protocol (NFS).

Color Touchscreen, Mouse, and Keyboard

Save time with the HP 16500B color touchscreen. Simply point to the field you want to change; the touchscreen eliminates the need to search a front panel for the right button. Pop-up menus offer all choices at a glance, and the software ensures that you always make a valid choice. Front-panel operations can also be executed with a mouse and/or keyboard providing complete user-interface flexibility.

Color discriminates between overlapped traces. In addition, you can customize for personal preference and environmental considerations. Even infrequent users spend less time making measurements and more time analyzing the results. With a push of a button the touchscreen can be disabled so you can point to the screen without activating it.

Store Setups and Data Quickly

It is easy to store and retrieve measurement results and setups with the built-in 86 MB hard disk drive or the 3½-inch floppy disk drive. Both disk drives are DOS compatible.

Standard Data Formats

Many HP 16500B measurement modules can store data listings as ASCII files so you can post-process data using common software packages such as Microsoft Excel. All screen images can be stored in industry-standard PCX or TIFF formats so you can document your measurements using numerous PC and workstation applications which import these file types.

RS-232C, HP-IB, and Ethernet

Program the 16500B with easily understood commands through built-in RS-232C and HP-IB interfaces. Or, use the 16500L interface card to control the instrument or access data and screen images over Ethernet.

With compliments

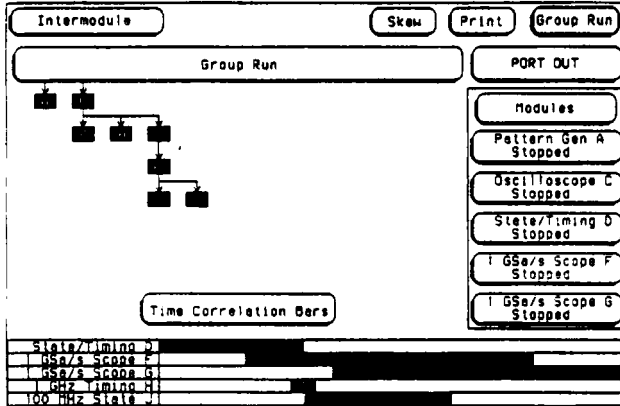
Helmut Singer Elektronik

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HP 16500B Intermodule Bus (IMB)

IMB Lets You Make Measurements Never Before Possible with One Instrument

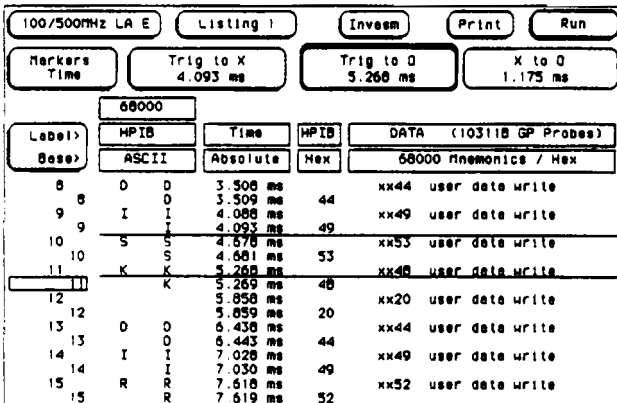
Run HP 16500 Series modules independently or combine their capabilities and correlate their acquisitions with 2 ns resolution to make measurements that previously required several instruments. The intermodule menu graphically communicates complex arming sequences in an easy-to-understand format. Use the time correlation bars for a quick overview of the measurements performed.



With the HP 16500 Series intermodule bus, you can arm or trigger one measurement module from another.

Analyze Systems with Multiple Microprocessors

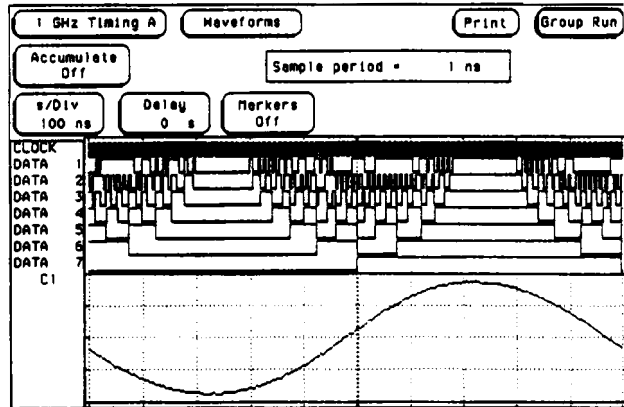
Capture states from separately clocked systems, such as multiple microprocessors or a microprocessor and a bus. Then analyze data flows between the systems with interleaved, time-correlated state displays.



Interaction of a 68000 microprocessor system and its HP-IB port.

Verify Mixed-Signal System Behavior

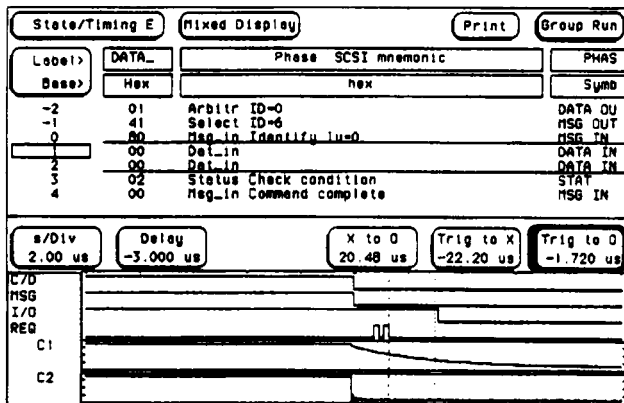
View the digital activity with up to 250 ps resolution in your mixed-signal system. Then display the time-correlated analog input signals captured with the built-in, 250 MHz digitizing oscilloscope to verify results.



Analog input signal correlated with its digitized output.

The Most Powerful Scope Trigger

Use the state analyzer to identify a problem sequence. Arm the timing analyzer with the state analyzer. Then arm the oscilloscope with the timing analyzer to capture a signal's parametric behavior at the exact time.



The state analyzer armed the timing analyzer, which then armed the built-in scope to capture a hard-to-find fall-time violation.

With compliments
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LOGIC ANALYZERS

State and Timing Analysis Modules

HP 16550A

Key Specifications and Characteristics

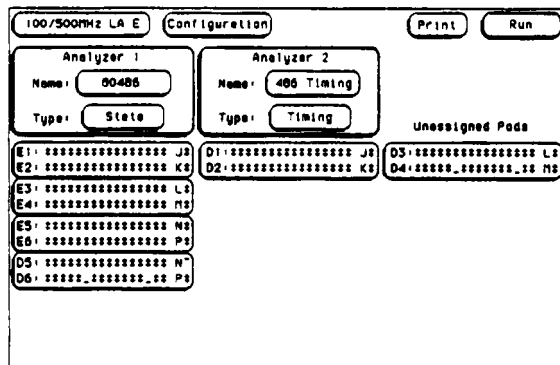
	HP 16550A ¹
Timing analysis rate	Conventional: 250/500 MHz ² Transitional: 125/250 MHz ² Glitch: 125 MHz
State analysis rate	100 MHz
Channels/card	102
Memory depth/channel	4 K/8 K
Setup/hold time	3.5/0 ns to 0/3.5 ns adj. in 500 ps steps
Minimum detectable glitch	3.5 ns
Probe input R and C	100 kΩ and ~8 pF
Trigger terms	Patterns: 10 Ranges: 2 Edge and glitch: 2 Timers: 2
Trigger sequence levels	12 in state and 10 in timing
Labels	126
Symbols	Unlimited with HP E2450A Symbol Utility, 1000 otherwise

¹ Two HP 16550A boards may be connected together for 204-channel operation.
² Half-channel mode doubles memory depth, doubles maximum conventional timing speed, and doubles maximum transitional timing speed.

State and Timing Analysis Modules

Capture State or Timing Data on All Channels

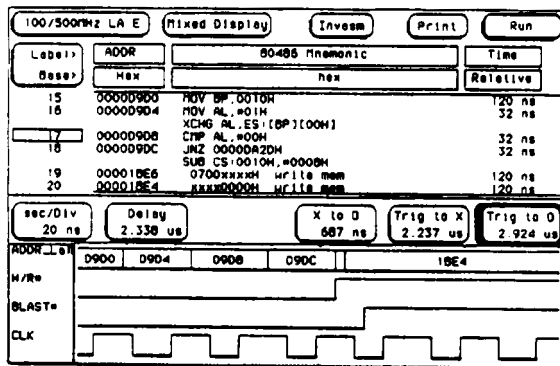
No need to connect special probes to view timing activity. All channels on HP state and timing analysis modules perform either state or timing. Set up your HP 16550A analyzer to perform simultaneous state analysis on some channels and timing analysis on the rest.



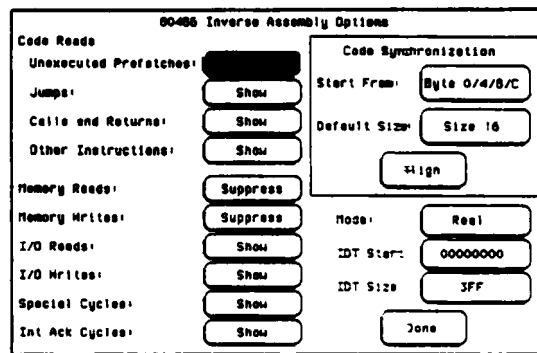
Assign channels to capture state or timing data without moving probes.

Find Whether the Problem Is in Software or Hardware

Arm the timing analyzer with the state analyzer to capture system behavior between states. Display both measurements on one screen and use time-correlated markers to identify the cause of problem states.



Display time-correlated state and timing measurements on the same screen.

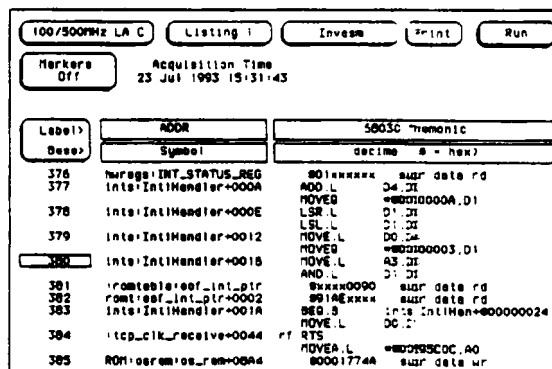


Disassembly filters let you analyze your software from multiple viewpoints.

Analyze Your Software with Informative Listings

New technology allows you to filter the disassembled trace, so it's easier to analyze. For example, suppress the display of instructions that were prefetched, but never executed.

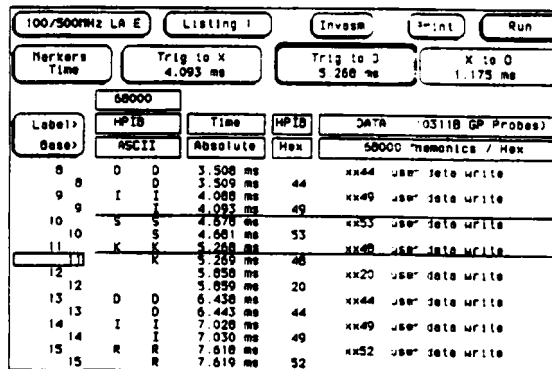
Display your high-level symbols in the state listing. If you program in a high-level language, the optional HP E2450A Symbol Utility lets you import symbols from your source code. The utility reads several industry-standard object module formats.



Debug using your high-level software symbols. The HP E2450A symbol utility lets you import and display symbols from your software code.

Track Problems in Multiprocessor Systems or Between the Processor and Its Interface Bus

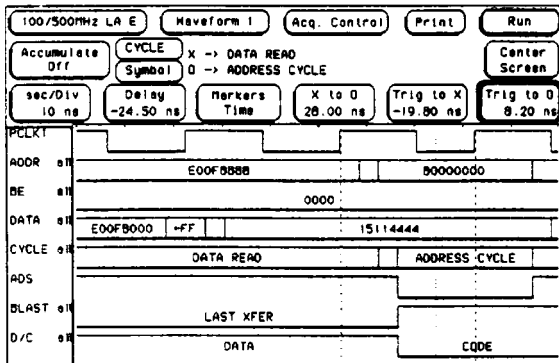
Configure your HP 16550A as two independent state analyzers that sample data using separate clocks. Time tagging of states lets you time-correlate and view the state listings interleaved on the same screen.



View interactions between two separately clocked systems.

Analyze Distant Timing Events with Transitional Timing

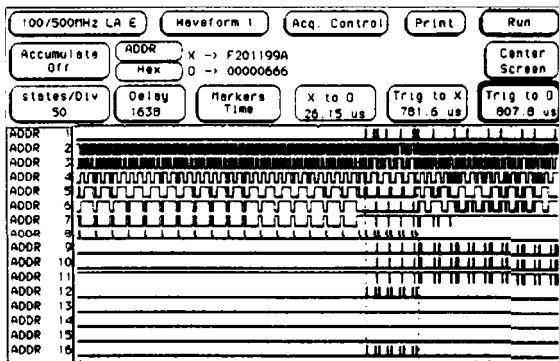
Capture events that are seconds apart maintaining up to 4 ns resolution with the HP 16550A. Transitional timing samples at full speed but only stores data when a transition occurs. This technique effectively extends the total time captured by the acquisition memory while maintaining high time resolution.



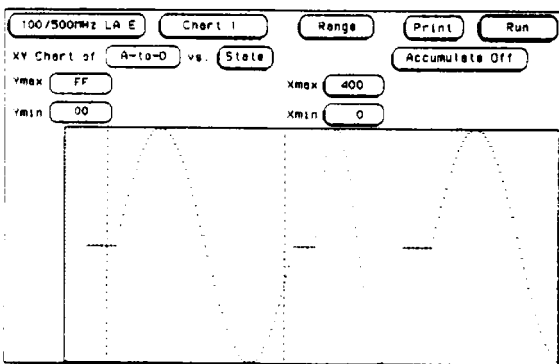
Display HP 16550A, 16542A, or 16517A/16518A, timing measurements with bus values overlaid in the waveforms.

Enhance Troubleshooting with Flexible Display Modes

State and timing analyzers let you display state measurements in listings, X-Y chart, or state waveforms. In addition to the waveform display, the HP 16550A, 16542A, and 16517A/16518A allow you to display timing information as a listing. Markers placed on one display are automatically updated in other display modes.



View entire state acquisition at a glance with state waveform



Verify the output of your A-D converter or DSP system with state X-Y chart display.

Find Intermittent Errors Using Postprocessing

In state, set up compare mode to "run until compare not equal" to capture intermittent errors. Use compare for quick go/no-go testing of your product in manufacturing. State compare shows you the effects of system changes by comparing each sample in the current measurement to each sample in a previous measurement.

In timing, capture intermittent setup and hold violations using the specify-stop-measurement feature to repetitively acquire data until the time interval between two patterns violates a specified condition.

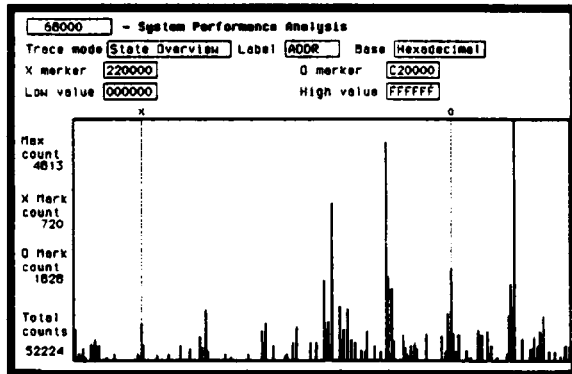
HP 10390A System Performance Analysis Software (HP 16550A, and 1660 Series)

Optimize Your System's Performance

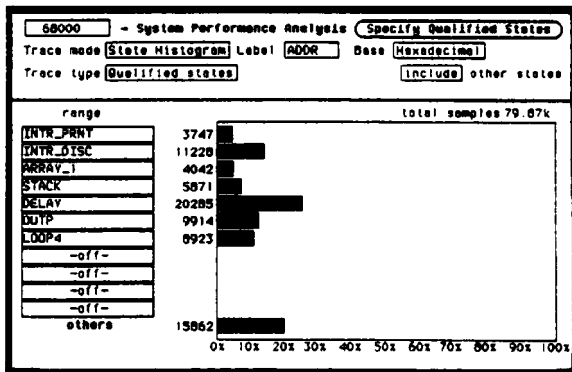
See an overall picture of your system. Find the routines that are slowing performance. Locate routines that are called most often, identify inefficient use of disks and peripherals, and find processes that use too much CPU time.

The HP 10390A system performance analysis software (SPA) converts your HP state analyzer into a powerful tool for finding bottlenecks in your system. SPA uses the state analyzer to sample your target system repetitively. The data captured is sorted into ranges before a new measurement is started after a random delay. After each acquisition, the captured information is translated into histograms and bar charts to present an accurate picture of your system's operation.

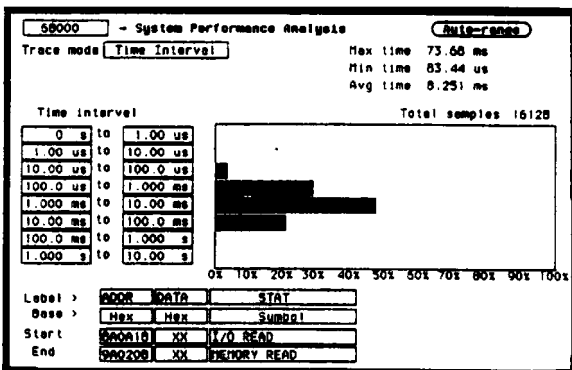
SPA performs three kinds of measurements: state overview, state histogram, and time interval measurements.



Use state overview mode as a coverage test for diagnostic software or to verify there are no accesses to protected memory segments.



Determine how often your system accesses specific routines. Use state histogram mode to characterize use of peripherals to optimize your system.



Characterize the speed of your software using time interval measurements. Find I/O routines that reduce system performance and measure their average, minimum, and maximum execution times.

LOGIC ANALYZERS

State and Timing Analysis Modules

HP 16542A and HP 16517A, 16518A



HP 16542A Deep Memory State and Timing Module

Collect and Analyze Large Streams of Data

The HP 16542A module provides high-speed, configurable, deep memory logic analysis for your HP 16500 Series system. Debug systems that process and transfer large streams of data, such as image processing systems, radar or other imaging systems, DSP systems, and telecommunications systems. Find the cause of intermittent system crashes by capturing up to 1 M of inverse-assembled states in your computer system. Perform benchmark testing and system performance analysis by acquiring up to 10 MB of data per run.

Key Specifications and Characteristics

HP 16542A	
Channels/card	16
Memory depth/channel/card	1 Mb/channels × 16 channels or 2 Mb/channels × 8 channels
Maximum memory depth/channel	1 Mb/channels × 80 channels 2 Mb/channels × 40 channels 5 Mb/channels × 16 channels* 10 Mb/channels × 8 channels*
Maximum state input clock rate	100 MHz
Timing analysis rate	100 MHz, fixed

*Requires HP E2430A memory expansion interface for multcard configurations.

Capture Entire Frames of Image Data

Capture and analyze image data from image processing systems, such as HDTVs, scanners, facsimiles, laser printers, and color photocopiers.

Label	ADDR	Symbol	Address (Hex)	Invasm (Decimal)
15409	absolute F00042	pF00042	LDI	--R3, R3
15410	absolute F00043	pF00043	LDI	--R3, R3
15411	absolute F00044	pF00044	LDI	--R3, R3
15412	absolute F00045	pF00045	LDI	--R3, R3
15413	absolute F00046	pF00046	LDI	--R3, R3
15414	absolute F00047	pF00047	LDI	--R3, R3
15415	absolute F00048	pF00048	LDI	--R3, R3
15416	absolute F00049	pF00049	LDI	--R3, R3
15417	absolute F0004A	pF0004A	LDI	--R3, R3
15418	absolute F0004B	pF0004B	LDI	--R3, R3
15419	absolute F0004C	pF0004C	LDI	--R3, R3
15420	absolute F0004D	pF0004D	LDI	--R3, R3
15421	absolute F0004E	pF0004E	LDI	--R3, R3
15422	absolute F0004F	pF0004F	LDI	--R3, R3
15423	absolute F00050	pF00050	LDI	--R3, R3
15424	absolute F00051	pF00051	LDI	--R3, R3

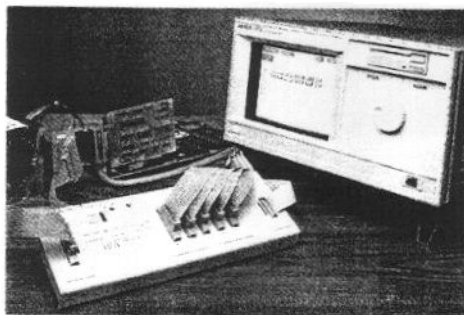
Capture up to 10 MB of data in a single acquisition.

Debug Digital Signal Processor Systems

Combine the HP 16542A with other HP 16500 Series modules for full DSP analysis in a single, easy-to-use mainframe. Use the HP 16550A 100-MHz state/timing analyzer to monitor code flow; the HP 16542A for memory-intensive data stream capture; and the HP 16532A 1-GSa/s oscilloscope for viewing parametric anomalies on the analog I/O streams.

Capture Data Bursts with Multirecord Mode

Use multirecord mode to specify a recurring trigger pattern and data stream length so that multiple data bursts or occurrences of real-time events may be captured in a single acquisition. Only data within these boundaries are stored, thereby using acquisition memory more effectively.



HP E2430A memory expansion interface allows one probe to drive up to five HP 16542A data acquisition cards for up to 10 Mb/channel memory depth.

HP 16517A/16518A High-Speed State and Timing Module

Make Time Measurements with the Resolution and Precision of an Oscilloscope

Key Specifications and Characteristics

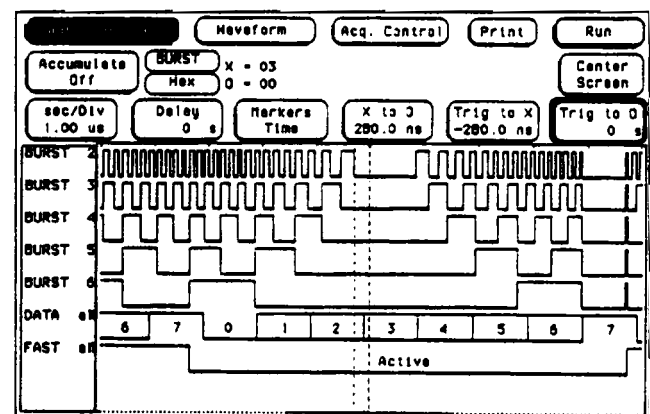
HP 16517A/16518A	
Maximum timing speed	2 GSa/s or 4 GSa/s*
Maximum state speed	1 GSa/s
Memory depth	64 K or 128 K*
Channels per card	16/16*
Probe input R&C	0.2 pF, then through 500 Ω, 3 pF and 100 KΩ
Trigger macro library	Yes, with 4 sequence levels
Channel-to-channel skew	250 ps, typical

*Half-channel mode doubles memory depth and doubles timing speed.

*HP 16518A expansion card requires HP 16517A master card. Up to four HP 16518As are supported by each HP 16517A.

Find the Cause of Elusive Problems

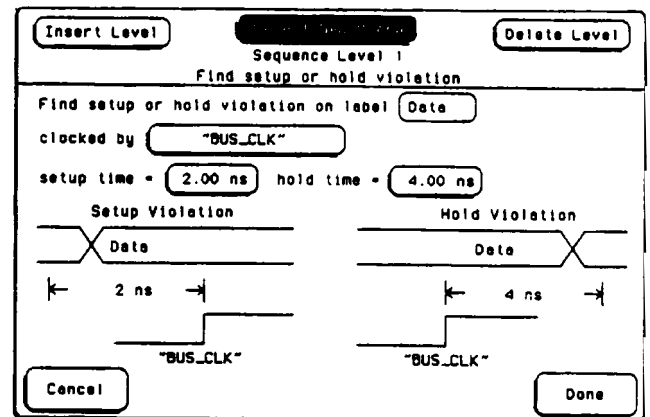
The 64 K deep memory lets you capture data over many clock cycles while retaining the highest multi-channel accuracy ever in a logic analyzer. Verify the timing of critical edges with 250 ps resolution across up to 40 channels, or 500 ps resolution, across up to 80 channels. Use the 1 GSa/s synchronous state analysis to view high-speed data streams across up to 80 channels.



Capture 32 μs of circuit activity while maintaining 250 ps resolution.

Precisely Characterize Setup or Hold Times

The 250 ps precision (channel-to-channel skew) allows this logic analyzer to be used in place of an oscilloscope for characterization. The high channel count of a logic analyzer makes this a much more efficient process.



A graphical trigger macro library ensures fast trigger condition setups.

HP 16532A Digitizing Oscilloscope

Built-in, Full-Featured Digitizing Oscilloscope

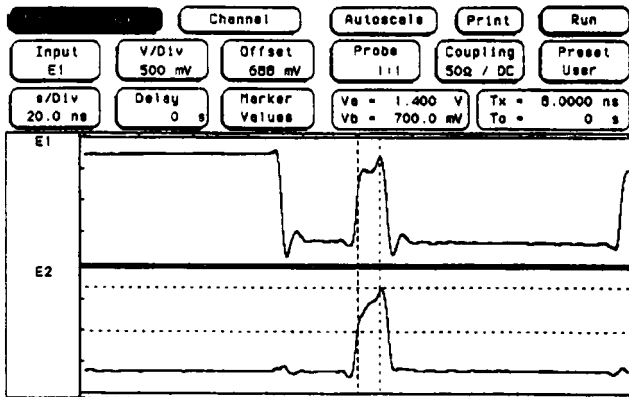
The HP 16532A offers the advantages of a full-featured color digitizing oscilloscope integrated into your logic analyzer. The HP 16532A offers digitizing advantages such as autoscale, automatic measurements, powerful triggering, negative time viewing, voltage markers, and time markers.

Key Specifications and Characteristics

	HP 16532A
Sample rate	1 GSa/s
Bandwidth ¹	250 MHz
Rise time ²	1.4 ns
Time interval accuracy	± 150 ps
ADC resolution	8 bits
Waveform record length	8000
Channels per card	2
Max. single time base channels	8
Max. channels per system	20

Use as a Standalone Scope with Many Channels

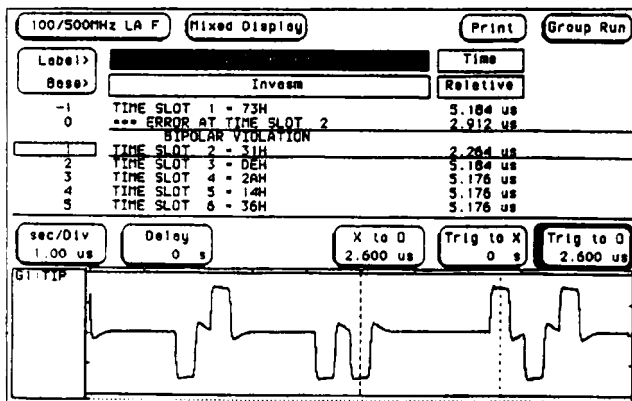
You can capture up to eight analog channels simultaneously (single time base). You can measure slow and fast events by adding additional oscilloscope modules to create a multiple time base digitizing oscilloscope. For large channel count measurements, you can configure as many as 20 HP 16532A scope channels in a single system.



Simultaneously view up to eight channels—individually or overlaid—to observe timing relationships.

Combine Scope with Other Logic Analysis Modules

You can arm or trigger the oscilloscope from any other module in the HP 16500 Series to capture and display the analog events that affect your digital system.



The state analyzer armed the built-in scope to capture a hard-to-find DS1 bipolar violation.

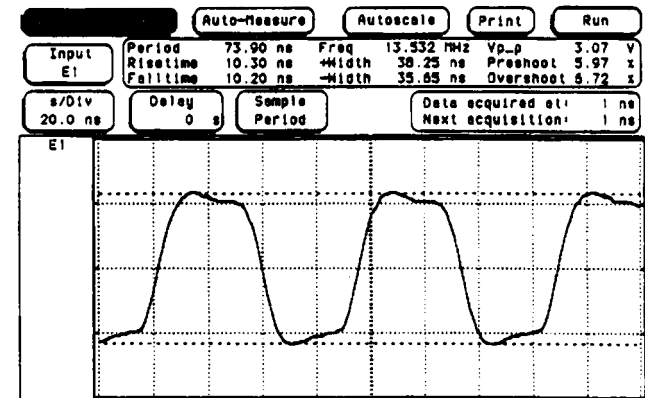
Autoscale, Auto-Measure, Voltage and Time Markers, and Color Save You Time

Select Autoscale and the scope adjusts the time, voltage, and trigger levels instantly for a stable display of your waveforms. Use automatic measurements to analyze a signal's behavior easily. Independent voltage and time markers can be used to measure voltage and timing relationships. Plus, automatic market placement and statistics allow you to characterize a circuit quickly.

Waveforms are independently colored for fast and easy identification.

Automatic measurements display:

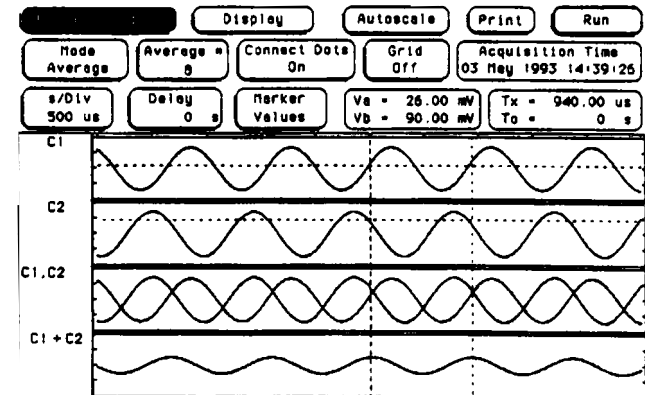
Period	Frequency	Peak-to-peak voltage
Rise time	+ Pulse width	Prehoot
Fall time	- Pulse width	Overshoot



Automatic measurements quickly identify a signal's parameters.

Flexible Display Modes Help You Find Signal Problems

Capture random signal variations or metastable states with the accumulate mode. Filter out noise with the average mode. Show true single-shot events with the single mode. Scan many periods of the waveform easily with the connect-the-dots feature. Analyze differential waveforms with the A-B mode.



Waveform math functions show relationships between measured

¹Specifications

²Rise time is calculated from: Rise time = 0.35/bandwidth

With compliments

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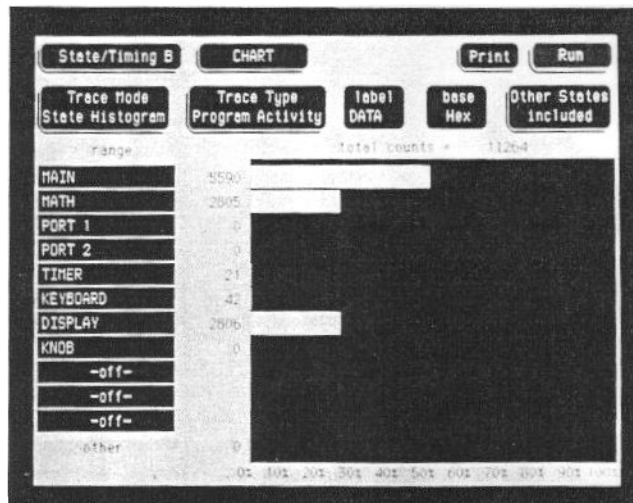
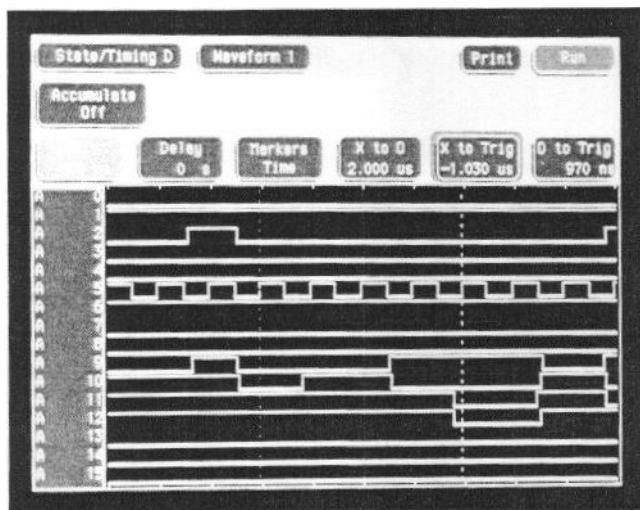
LOGIC ANALYZERS

Logic Analyzer-on-a-Card

Model 16510A

- 80 channels of 25 MHz state or 100 MHz timing
- Transitional timing for deep effective memory
- Configure up to 400 channels

- Debug multiple 32-bit microprocessor systems
- Supports 8-, 16-, and 32-bit microprocessors
- Lightweight passive probing



HP 16510A Logic Analyzer ... an HP 1650A on a card*

Number of Channels 80 channels per card, up to 400 channels in one HP 16500A.

Types of Analysis	25 MHz state, 100 MHz timing, simultaneous state/state, simultaneous state/timing.
Glitch Detection	5 ns minimum pulse width between samples; trigger on and/or capture on all channels.
Marker Measurements	Time interval; number of states; pattern search; minimum, maximum, and average time interval statistics.
Timing Violation Measurements	Acquire data until time interval between two specified patterns violates a specified condition.
System Performance Analysis	State label, time interval, state overview; requires HP 10390A.
Data Display/Entry	Binary, octal, decimal, hexadecimal, ASCII (display only), user-defined symbols.
Deep Effective Memory	Uses transitional timing to store data only when there is a transition.
Debug Modes	Overlap mode allows viewing of timing violations. Infinite persistence shows waveform changes during repetitive acquisitions.
Triggering and Pattern Qualification	Duration, glitch, or edge specify error conditions, 8 sequence levels, 8 pattern recognizers, 1 range recognizer, state armed timing or timing armed state.
Small Lightweight Probing	100 kohm; 8 pF; individually grounded; 2 x 10, .1" center connectors.
Microprocessor Support	Most popular 8-, 16-, and 32-bit microprocessors.
Data Qualification	5 clock inputs, 4 clock qualifiers, storage qualification, time and number of state tagging, pre-store.
Interactive Measurements	Configure each HP 16510A module as two independent state analyzers, or one state and one timing analyzer.

*Refer to the HP 1650A section for more information on the HP 16510A's capabilities.

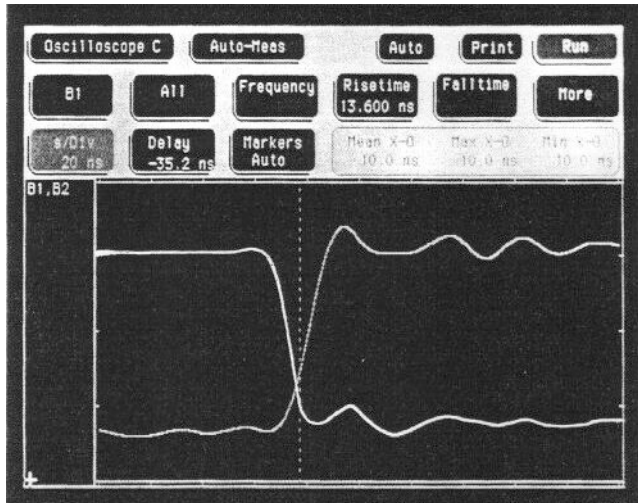
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 Feldchen 16-24 D-52070 Aachen Germany

- 400 Megasamples/s single-shot analysis
- Better than 1 ns time interval accuracy (single-shot)
- Up to 8 simultaneous oscilloscope channels



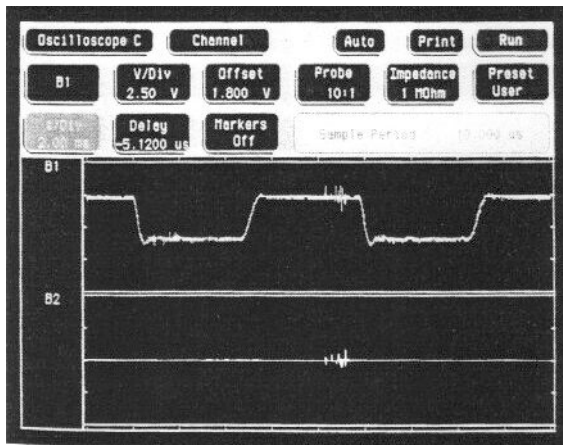
HP 16530A/16531A Digitizing Oscilloscope . . . Capture and Time Correlate Single-shot Events Precision Time Interval Measurements

Make time interval measurements with markers at better than 1 ns accuracy single-shot (after deskewing). Accuracy at the probe tip is assured by a calibration routine that reduces channel-to-channel skew.



Single-shot Analysis

The HP 16531A 2 channel, 400 megasamples/s digitizing oscilloscope captures 100 MHz bandwidth signals single-shot. Multiple channels can be captured simultaneously so that you can determine relationships between infrequent events. A high-resolution color display and post-capture scroll and zoom allow you to examine waveforms in detail.



Capture Many Waveforms Simultaneously

Run up to four HP 16531A oscilloscope cards with a single HP 16530A timebase card for simultaneous acquisition. Your HP 16530A/16531A oscilloscope module can be configured to acquire from two to eight signals simultaneously. Save time when debugging and characterizing systems by observing multiple test points during each test.

- 4 ksamples memory depth/channel for pre-trigger debugging
- Oscilloscope triggered by logic analyzer
- Automatic measurement and setup aids

Measure Slow and Fast Events Simultaneously

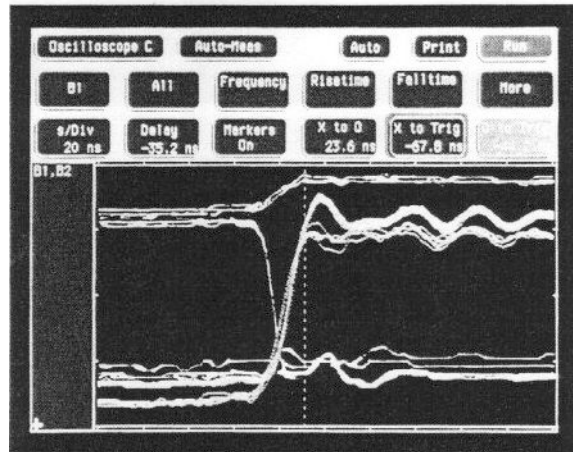
Use the 4K memory depth to measure periods and time intervals; then zoom in for risetime measurements. Add a second oscilloscope module to create a dual timebase digitizing oscilloscope.

Find the Causes of Errors

Each channel has 4K memory depth for capturing events before or after the trigger event. View events up to 10 us before the trigger event with greater than 1 ns accuracy.

View Analog and Digital Waveshapes . . . and More

Capture random signal variations with Accumulate mode. Filter out noise with Average mode. Show true single-shot events with Single mode. Scan many periods of the waveform easily with Connect-the-dots. View analog-like waveshapes with 6 bit vertical resolution. Analyze differential waveshapes with the A-B mode.



Automatic Measurements

Automatic pulse parameters allow fast analysis without having to count gratitudes. Parameters such as frequency, period, pulse width, peak-to-peak voltage, maximum voltage, minimum voltage, risetime, falltime, preshoot, and overshoot are just one keystroke away. Also measure voltage and timing relationships by placing the markers and reading the answer on the display. Display the time between markers, acquire until capturing specified time between markers, perform statistical analysis on the time between markers. Setup is easy with automatic waveform scaling, TTL & ECL presets aid scaling, and automatic marker placement on specified edges.

With compliments
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LOGIC ANALYZERS

1 GHz Timing Analyzer-on-a-Card

Model 16515A, 16516A

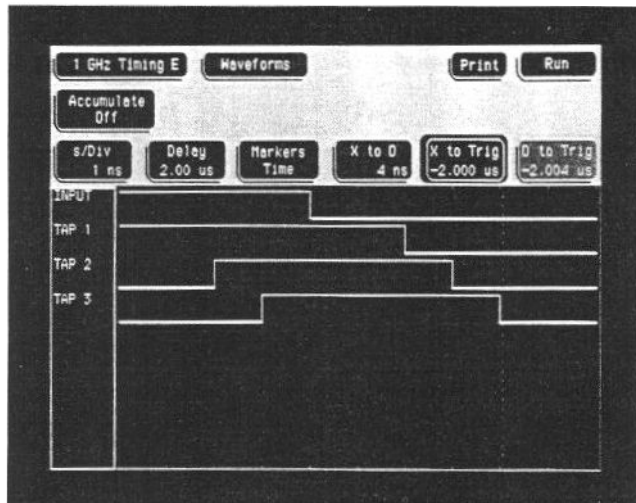
- 1 GHz timing for 1 nanosecond resolution
- 16 channels/card for up to 80 channels/frame
- 8 Kbits per channel memory depth



HP 16515A/16516A ... Capture High-speed Events with 1 Gigahertz Timing

Measure Time Intervals Precisely with 1 ns Resolution

Measure precise time relationships on high speed TTL, CMOS, and ECL circuits with 1 ns single-shot resolution.



Debug Quickly with up to 80 Channels

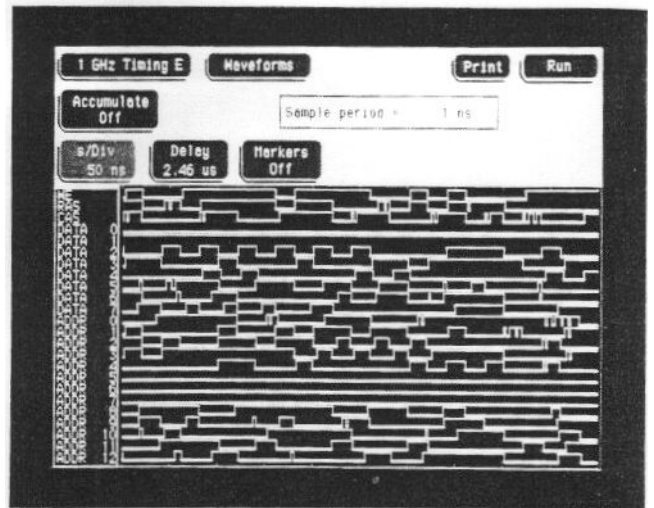
Avoid having to move probes. Find problems faster by capturing more channels at the same time, and solve applications that require several simultaneous channels. Each HP 16515A/16516A timing card offers 16 simultaneous channels. Add up to five cards for a total of 80 channels for applications where having more channels means taking less time to find the problem.

With compliments

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- Lightweight passive probing
- Easy-to-use scope-like controls



Find the Cause of Problems with 8 Kbit/channel Memory Depth

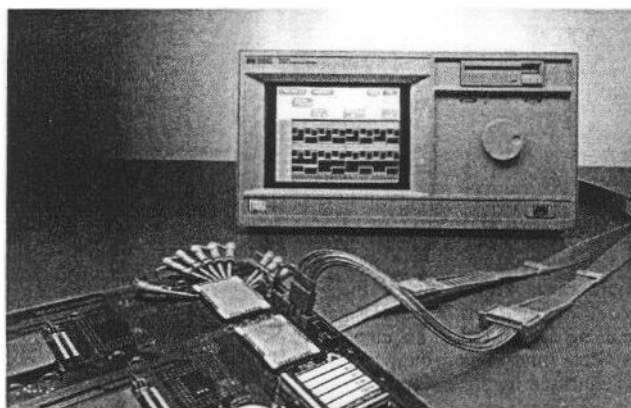
Find and analyze events that occur before or after the trigger event. Each channel stores 8K samples to allow 8 us of negative time capture with 1 ns resolution, for pre-trigger applications. Deep memory stores data over several clock cycles while retaining precise edge placement information. Deep memory also helps you find elusive problems more quickly when you're not sure exactly where to trigger.

Hook Up Easily to Your Circuit with HP's New Lightweight Probes

HP's new 50 kohm, 2 pF passive probes are lightweight and easy to connect. These probes are color-coded and can be connected with probe tips or plugged directly into any .1" grid with .026" to .033" diameter round pins or .025" square pins. Individual grounds are provided for each channel to shorten ground loops.

Easy-to-use

Enjoy the HP 16515A/16516A timing module's scope-like controls by selecting seconds/division and delay. Automatic pattern search quickly finds patterns. Statistical time interval analysis measures the dynamics of your circuits.



LOGIC ANALYZERS

Specifications And Characteristics

Models 1650A, 1651A, 16500A, 16510A, 16515/16A, 16520A/21A, 16530A/31A

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HP 1650A, 1651A, 16510A Specifications

Probes

Minimum Swing: 600 mV peak-to-peak.

Threshold Accuracy: ± 150 mV accuracy over the range -2.0 to 2.0 volts; ± 300 mV accuracy over the ranges -9.9 to -2.1 volts and 2.1 to 9.9 volts.

Dynamic Range: ± 10 volts about the threshold.

State Mode

Clock Repetition Rate: Single phase is 25 MHz maximum. With time or state counting, minimum time between states is 60 ns. Both mixed and demultiplexed clocking use master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede the next slave clock by > 50 ns.

Clock Pulse Width: ≥ 10 ns at the threshold.

Setup Time: Data must be present prior to clock transition, ≥ 10 ns.

Hold Time: Data must be present after rising clock transition, 0 ns.

Timing Mode

Minimum Detectable Glitch: 5 ns wide at the threshold.

Characteristics

Probes

Input RC: 100 K Ω $\pm 2\%$ shunted by approximately 8 pF at the probe tip.

Minimum Input Overdrive: 250 mV or 30% of the input amplitude, whichever is greater.

Maximum Voltage: ± 40 volts peak.

Threshold Setting: Threshold levels may be defined for pods 1 and 2 individually (HP 1651A). Threshold levels may be defined for pods 1, 2, and 3 on an individual basis and one threshold may be defined for pods 4 and 5 (HP 1650A/16510A).

Threshold Range: -9.9 to $+9.9$ volts in 0.1 volt increments.

State Analysis

Memory

Data Acquisition: 1024 samples/channel

Trace Specification

Clock: Five clocks (HP 1650A/16510A) or two clocks (HP 1651A) are available and can be used by either one or two state analyzers at any time. Clock edges can be ORed together and operate in single phase, two phase demultiplexing, or two phase mixed mode. Clock edge is selectable as positive, negative, or both edges for each clock.

Clock Qualifier: The high or low level of four clocks (HP 1650A/16510A) or one clock (HP 1651A) can be ANDed with the clock specification. Setup time: 20 ns; hold time: 5 ns.

Pattern Recognizers: Each recognizer is the AND combination of bit (0, 1, or X) patterns in each label. 8 pattern recognizers are available when one state analyzer is on. 4 are available to each analyzer when two state analyzers are on.

Range Recognizer: Recognizes data which is numerically between or on two specified patterns (ANDed combination of zeros and/or ones). One range term is available and is assigned to the first state analyzer turned on. The maximum size is 32 bits.

Qualifier: A user-specified term that can be anystate, nostate, a single pattern recognizer, range recognizer, or logical combination of pattern and range recognizers.

Sequence Levels: There are 8 levels available to determine the sequence of events required for trigger. The trigger term can occur anywhere in the first 7 sequence levels.

Branching: Each sequence level has a branching qualifier. When satisfied, the analyzer will restart the sequence or branch to another sequence level.

Occurrence Counter: Sequence qualifier may be specified to occur up to 65535 times before advancing to the next level.

Storage Qualification: Each sequence level has a storage qualifier that specifies the states that are to be stored.

Enable/disable: Defines a window of post-trigger storage. States stored in this window can be qualified.

Prestore: Stores two qualified states that precede states that are stored.

Tagging

State Tagging: Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Maximum count is 4.4×10^{12} .

Time Tagging: Measures the time between stored states, relative to either the previous state or to the trigger. Maximum time between states is 48 hours. With tagging on, the acquisition memory is halved; minimum time between states is 60ns.

Symbols

Pattern Symbols: User can define a mnemonic for the specific bit pattern of a label. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs. Bit patterns can include zeros, ones, and don't cares.

Range Symbols: User can define a mnemonic covering a range of values. Bit pattern for lower and upper limits must be defined as a pattern of zeros and ones. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.

Number of Pattern and Range Symbols: 100 per analyzer. Symbols can be down-loaded over RS-232C.

Timing Analysis

Transitional Timing Mode: Sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.

Sample Period: 10 ns

Maximum Time Covered by Data: 5000 seconds

Minimum Time Covered by Data: 10.24 us

Glitch Capture Mode: Data sample and glitch information is stored every sample period.

Sample Period: 20 ns to 50 ms in a 1-2-5 sequence dependent on sec/div and delay settings.

Time Covered by Data: Sample period \times 512

Waveform Display

Accumulate: Waveform display is not erased between successive acquisitions.

Overlay Mode: Multiple channels can be displayed on one waveform display line. Primary use is to view summary of bus activity.

Maximum Number of Displayed Waveforms: 24

Time Interval Accuracy

Sample Period Accuracy: 0.01% of sample period.

Channel-to-channel Skew: 4 ns typical

Time Interval Accuracy: \pm (sample period + channel-to-channel skew + 0.01% of time interval reading)

Trigger Specification

Asynchronous Pattern: Trigger on an asynchronous pattern less than or greater than specified duration. Pattern is the logical AND of specified low, high or don't care for each assigned channel. If pattern is valid but duration is invalid, there is a 20 ns reset time before looking for patterns again.

Greater than Duration: Minimum duration is 30 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Accuracy is $+0$ ns to -20 ns. Trigger occurs at pattern + duration.

Less than Duration: Maximum duration is 40 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Pattern must be valid for at least 20 ns. Accuracy is $+20$ ns to -0 ns. Trigger occurs at the end of the pattern.

Glitch/Edge Triggering: Trigger on glitch or edge following valid duration of asynchronous pattern and while the pattern is still present. Edge can be specified as rising, falling or either. Less than duration forces glitch and edge triggering off.

Measurement And Display Functions

Autoscale (Timing Analyzer Only): Autoscale searches for and displays channels with activity on the pods assigned to the timing analyzer.

Acquisition Specifications

Arming: Each Analyzer can be armed by the Run key, the other Analyzer, the external trigger in port (HP 1650A/1651A) or the Inter-module Bus (HP 16500A).

Trace Mode: Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until stop is pressed or until time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range. There is only one trace mode when two analyzers are on.

Labels: Channels may be grouped together and given a 6-character name. Up to 20 labels in each analyzer may be assigned with up to 32 channels per label. Primary use is for naming groups of channels such as address, data, and control busses.

Indicators

Activity Indicators: Provided in the Configuration, State Format, and Timing Format menus for identifying high, low, or changing states on the inputs.

Markers: Two markers (X and O) are shown as dashed lines in the display.

Trigger: Displayed as a vertical dashed line in the timing waveform display and as line 0 in the state listing display.

Marker Functions

Time Interval: The X and O markers measure the time interval between one point on a timing waveform and trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).

Delta States (State Analyzer Only): The X and O markers measure the number of tagged states between one state and trigger, or between two states.

Patterns: The X or O marker can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The O marker can also find the nth occurrence of a pattern before or after the X marker.

Statistics: X to O marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to O time, maximum X to O time, average X to O time, and ratio of valid runs to total runs.

HP 16530A/16531A 400 Megasample/s Digitizing Oscilloscope

Specifications

Vertical (at BNC)

Bandwidth (-3 dB): dc to 100 MHz (dc-coupled)

Range: 40 mV to 16 V full scale (adjustable with 2-digit resolution).

DC Gain Accuracy: ±3% of full scale (valid within ±10°C of auto-calibration temperature)

Analog-to-digital Conversion (ADC) Resolution: ±1.6% of full scale (6 bits)

DC Offset Accuracy: ±1% of offset ±3.2% of full scale (valid within ±10°C of auto-calibration temperature).

DC Offset Range/Resolution:

Vertical Range	Offset Range	Offset Resolution
<800 mV	±800 mV	1 mV
≥800 mV	±16 V	20 mV

Voltage Measurement Accuracy (DC):

Single Cursor (X or O): = Gain accuracy + ADC resolution + offset accuracy.

Dual Cursor (X to O measurements on the same waveform): = Gain accuracy + 2 (ADC resolution)

Horizontal

Range: 50 ns to 100 s full scale, adjustable with 3-digit resolution.

Time Interval Measurement Accuracy (dual channel for deskewed channels with equal rise and fall times):

±0.75 ns ±0.2% of timebase range ±0.02% of reading (2.5 ns sample period)

± sample period ±0.2% of timebase range ±0.02% of reading (≥ 5 ns sample period)

Delay (Time Offset)

Pre-trigger Range: 4096 × sample period

Post-trigger Range: 500 screen diameters

Resolution: Fine adjustment to 0.2% of screen diameter

Characteristics

Vertical

Transition Time (10% to 90%): ≤ 3.5 ns

Input Coupling: dc

Input RC: 1 MΩ ±2% or 50 ohm ±3%, shunted by approximately 13 pF.

Maximum Safe Input Voltage: 1 MΩ input, ±40 V (dc + peak ac), 50 Ω input, ± 5 V (dc + peak ac)

Probe Factors: Any integer ratio from 1:1 to 1:1000, to scale the oscilloscope to represent voltages seen at the probe tip.

Time Base

Deskewing: Skew between channels can be nulled out to compensate for probe cable lengths.

Digitizer

Resolution: 6 bits (1 part in 64)

Digitizing Rate: up to 400 megasamples/second

Digitizing Technique: Real-time digitizing; each 4K record is acquired on a single acquisition.

Acquisition Memory Size: 4096 samples per channel

Waveform Display

Display Formats: Waveforms can be displayed in an overlapping and/or non-overlapping format.

Display Resolution: 500 points horizontally.

Display Modes

Single: New acquisitions replace old acquisitions on screen.

Accumulate: New acquisitions are added to the screen and displayed with older acquisitions until screen is erased.

Average: New acquisitions are averaged with older acquisitions with updated waveform displayed until erased.

Overlay: Up to 8 acquired waveforms can be overlaid in the same display area.

Connect-the-dots: Provides a display of the sample points connected by straight lines.

Waveform Reconstruction: When there is insufficient data to fill every horizontal location, a post-acquisition reconstruction filter fills in the missing locations.

Waveform Math: Display capability of A-B and A+B functions is provided.

Measurement Aids

Markers: Two vertical markers are provided for measurements of time and voltage. Capabilities are: measure voltage of X and O on each analog waveform; measure time from X to trigger, O to trigger, and X to O; automatic marker placement by specifying voltage level, edge number, and rising or falling edge type; run until X to O greater than, less than, in-range, and not-in-range provides selective event search; X to O statistics (mean, max, and min) provide analysis of time interval deviation.

Automatic Measurements: The following pulse parameter measurements can be performed automatically:

Frequency	Rise time	+ pulse width
Period	Fall time	- pulse width
Vpp	Preshoot	V _{top-base}
	Overshoot	

Setup Aids

Auto: Auto sets the vertical and horizontal ranges, offset, and trigger level to display the input signals. Requires an amplitude above 10 mV peak, and a frequency between 50 Hz and 100 MHz.

Presets: Scale the vertical range, offset, and trigger level to predetermined values for displaying ECL or TTL waveforms.

LOGIC ANALYZERS

Specifications And Characteristics (cont'd)

Models 1650A, 1651A, 16500A, 16510A, 16515/16A, 16520A/21A 16530A/31A

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HP 16515A/16516A 1 GHz Timing Analyzers

Specifications

Probes

Minimum Swing: 600 mV peak-to-peak.
Threshold Range: -3.5 to +5.0 volts in 0.1 volt increments.
Threshold Accuracy: ± 125 mV $\pm 2.5\%$
Dynamic Range: ± 7.0 volts

Timing Accuracy

Timing Accuracy: ± 1 Sample Period + Sample Rate Accuracy
 $\pm (300$ ps within a pod, 1 ns between pods)
Sample Rate Accuracy: $\pm 0.01\%$ of measurement added to;
 ± 300 ps at 1 GHz
 ± 400 ps at 250 MHz and 500 MHz
 ± 800 ps at 125 MHz
 ± 1.6 ns at ± 62.5 MHz

Characteristics

Probes

Input RC: 50 K Ω $\pm 2\%$ shunted by ≤ 3 pF at the probe tip.
Minimum Input Overdrive: 250 mV or 25% of the input amplitude, whichever is greater.
Maximum Input Voltage: ± 40 volts.

Symbols

Pattern Symbols: User can define a mnemonic covering a range of values. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs. Bit patterns can include Zeros, Ones, and Don't Cares.

Range Symbols: User can define a mnemonic covering a range of values. Bit pattern for lower and upper limits must be defined as a pattern of Zeros and Ones. When data display is SYMBOL, values within the specified range are displayed as mnemonic \pm offset from base of range.

Number of Available Pattern and Range Symbols: 200 symbols can be down-loaded from controller.

Labels: Up to 20 labels may be assigned channels in any configuration up to 32 channels per label. Primary use is for naming groups of channels such as address, data, and control busses.

Indicators

Activity Indicators: Provided in the format menu for identifying high, low, or changing states on the inputs.

Markers: Two markers (X and 0) are shown as dashed lines in the display.

Tracepoint: Displayed as vertical dashed line in the waveform display. Defined as trigger + delay.

Marker Functions

Time Interval: The X and 0 markers measure the time interval between one point on a timing waveform and trigger, two points on the same timing waveform, or two points on different waveforms.

Pattern Search: The X and 0 marker can be used to locate a specified pattern.

Statistics: X to 0 marker statistics are calculated for repetitive full-memory acquisitions. Pattern must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition (i.e., a hit). Statistics are minimum X to 0 time, maximum X to 0 time, number of hits and number of acquisitions.

HP 16520A/16521A 50 Mbit/s Pattern Generator

Specifications

Clock Sources (16520A Only)

Internal Clock

Clock Period: programmable from 20 ns to 200 μ s in a one-two-five sequence.

Data Period Accuracy: $\pm 2\%$ (of period) ± 1 ns

External Clock (provided by user)

Input Clock Period: 1 Hz to 50 MHz (20 ns min period) ECL or TTL, internal frequency divide (/1, /5, or /10) provided.

Duty Cycle: 10 ns minimum high time, 10 ns minimum low time

Strobes (16520A Only)

Number of Strobes: 3 (ECL or TTL)

Bits/Channel: 4095

Maximum Bit Rate: 20 MBit/s (50 ns Period)

Edge Placement: ≤ 10 MBit/s: tenths of period

> 10 MBit/s to 20 MBit/s: fifths of Period

(Delay + Width \leq Period)

Minimum Delay: 0/10 (0/5), maximum delay is 9/10 (4/5) data period.

Minimum Width: 1/10 (1/5) of data period, maximum width is the data period (values in parentheses apply to 20 MBit/s timebase setting). If strobes are desired while operating with external clock, the data rate will be divided to 1/5 or 1/10 the external clock rate.

Characteristics

or TTL levels. All characteristics are valid at the probe tip.

	ECL	TTL
V_{OH} (steady state)	-0.98V	2.7V
V_{OL} (steady state)	-1.55V (into 10K Ω , 10 pF)	0.6V (into 10K Ω , 10 pF)
Risetime/ Falltime (typ)	2.3 ns (-0.98 V to -1.55 V)	2.5 ns (0.6 V to 2.7 V)
Channel-to- channel Skew* (same card)	≤ 5 ns	≤ 5 ns
Channel-to- channel Skew* (card-to-card)	< 10 ns	< 10 ns
Number of Std Loads	3 (10 KH ECL, @ $V_{nh}=150$ mV)	3 (LS, @ $V_{nl}=250$ mV)

(* Skew measured at (+1.6 V) TTL and (-1.3 V) ECL levels.

DATA CAPACITY	16520A	16521A
Number of Channels	12	48
Bits Per Channel	4095	4095
Maximum Bit Rate	50 MBit/s NRZ (20ns Period)	50 MBit/s NRZ (20ns Period)
INPUT	ECL	TTL
V_{ih} (min)	-0.91V	2.08V
V_{il} (max)	-1.69V	1.12V

Maximum Input Voltage: ± 40 V

Input Impedance: 100 K Ω , 8 pF

External Clock-in to Clock-out Delay: 50 ns

Data Instruction Set

Break: Stops program execution, last data vector is held at output.

Repeat: Repeats vector up to 256 times.

Wait IMB: Wait for intermodule trigger.

Wait External: Wait for user-defines 3-bit pattern on external input pod to become true. No data cycle latency when pattern is true between 30 ns and 0 ns before next clock edge.

Signal IMB: Arms other measurement cards.

Macro: Four different macros may be defined and inserted as needed. Six character labels may be defined for each macro. Macros contain REPEAT, WAIT EXTERNAL, WAIT IMB, BREAK, and SIGNAL IMB instructions.

General Characteristics

Auxiliary Power Available Through Cables:

HP 1650A/1651A/16510A: 2/3 amp @ 5V per cable; 2 amp @ 5V per HP 1650A/1651A/16510A; 16.3 amp-current draw of installed cards @ 5V per HP 16500A.

Current draw per card (@ 5V): 3.0 amp per HP 16510A, 1.3 amp per HP 16515A, 1.4 amp per HP 16516A, 0.7 amp per HP 16520A, 0.8 amp per HP 16521A, 0.4 amp per HP 16530A, 1.1 amp per HP 16531A.

Programmability: Instrument settings and operating modes, including automatic measurements, may be remotely programmed via RS-232C or HP-IB (IEEE-488). HP-IB is available only on HP 16500A.

Hardcopy Output

Printers Supported: HP ThinkJet, HP QuietJet, HP LaserJet, Epson and Epson-compatible printers (e.g., Epson FX80) via RS-232C or HP-IB (HP 16500A only).

RS-232C Configurations: Protocol: XON/XOFF, Hardware; Data bits: 7, 8; Stop bits: 1, 1½, 2; Parity: none, odd, even; Baud rate: 110, 300, 600, 1200, 2400, 4800, 9600, 19200.

Ordering Information

Logic Analyzers

HP 1631A (35 channels, plus two analog)
HP 1631D (43 channels, plus two analog)
HP 1650A (80 channels)
HP 1651A (32 channels)
HP 16500A Logic Analysis System
HP 16510A (80 channels)
HP 16515A (16 channels, 1 GHz timing)
HP 16516A (16 channels, 1 GHz timing)
HP 16520A (12 channels, pattern generation)
HP 16521A (48 channels, pattern generation)
HP 16530A (400 MSa/s oscilloscope timebase)
HP 16531A (400 MSa/s oscilloscope acquisition)

Probe Interface

HP 10269C G.P. Probe Interface
Microprocessor Preprocessors-note, inverse assembly is provided on 3.5-inch disc

HP 10304B Intel 8085
HP 10305B Intel 8086/88
HP 10306B Intel 80186/88
HP 10312D Intel 80286
HP 10314B Intel 80386
HP 10307B Motorola 6800/02
HP 10308B Motorola 6809/09E
HP 10310B Motorola 68008
HP 10311B Motorola 68000/10, 64-pin DIP
HP 10311G Motorola 68000/10, 68-pin PGA
HP 10313G Motorola 68020
HP 10303B National NSC800
HP 10300B Zilog Z80

Bus Preprocessors

HP 10342B HP-IB, RS-232C and RS-449
HP 10342G HP-IB

Minicomputer Interfaces

HP 10275A PDP-11 UNIBUS**
HP 10276A LSI-11 Q-Bus**
HP 52126A Intel Multibus***

Accessory Software

HP 10390A System Performance Analysis

User-Definable Interface

HP 10320C User-definable Interface
HP 10321A Microprocessor Interface Parts Kit
HP 10322A 40-pin DIP Interface Cable
HP 10323A 48-pin DIP Interface Cable
HP 10324A 64-pin DIP Interface Cable
HP 10391A Inverse Assembler Development Package

Printers and Accessories

HP 2225A ThinkJet Printer with HP-IB Interface
HP 10833A HP-IB Cable, 1m
HP 2225D ThinkJet Printer with RS-232C Interface
13242-60010 RS-232C Cable
HP 92261A Print Cartridge
HP 92261N Jet Paper (2500 Sheets, fanfold)
HP 92261S Mini-printer Stand

Oscilloscope Accessories

HP 10503A BNC-to-BNC cable, 1.2m
HP 10017A 10:1, 1 Mohm, 8 pF miniprobe, 1m
HP 10018A 10:1, 1 Mohm, 10 pF miniprobe, 2m
HP 10020A 10:1, 100:1, 10 Mohm, 10 pF resistive divider probe set, 1.5m
HP 10021A 1:1, 36 pF, mini-probe, 1m
HP 10022A 1:1, 62 pF, mini-probe, 2m
HP 10026A 1:1, 50 ohm, mini-probe, 1m
HP 10027A 1:1, 50 ohm, mini-probe, 2m
HP 10032A 100:1, 3 Mohm, 3 pF mini-probe, 1m
HP 10240B BNC-to-BNC AC coupling capacitor
HP 10211A 24-pin IC test clip

Logic Analyzer Accessories

01650-61607 16-Channel Probe Cable for HP 1650A and HP 1651A
16510-61601 16-Channel Probe Cable for HP 16510A
16515-61602 8-Channel Probe Cable for HP 16515A and HP 16516A
01650-61608 16-Channel Lead Set for HP 1650A, HP 1651A and HP 16510A (grey tip)
16515-62102 8-Channel Lead Set for HP 16515A and HP 16516A (blue tip)
01650-63201 Termination Adaptor for HP 1650A, HP 1651A and HP 16510A

5959-0288 Grabbers (package of 20)

Pattern Generator Accessories

16520-61601 Input qualifier Probe Cable
16520-61602 8-Channel Data Probe Cable
16520-61603 Clock Probe Cable
HP 10347A Pattern Generator Probe Lead Set
16520-69501 Input Qualifier Probe Kit
HP 10345A 8-Channel ECL Differential Driver Pod
HP 10346A 8-Channel TTL Tristate Buffer Pod
5959-0288 Grabber (package of 20)

Other Accessories

HP 1008A Option 006 Testmobile
1540-1066 Soft Carrying Case (for HP 1650A and HP 1651A)
HP 46060A HP Mouse (for 16500A only)
HP 92192A Black double-sided 3.5" microfloppy discs (box of 10)
5061-6175 HP 1650A & HP 1651A Rackmount Kit
5061-9679 HP 16500A Rackmount Kit
9211-2658 HP 16500A Transit Case
9211-2645 HP 1650A & 1651A Transit Case

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***Multibus is a trademark of Intel Corporation.

Agilent 16500, 16700, and 16900 Mainframe/Module Compatibility Matrix

	16500A	16500B	16500C	16505A	16600A-series	16700A-series	16700B-series	16900A-series
16510A	Yes	Yes	Yes	No	No	No	No	No
16510B	Yes	Yes	Yes	No	No	No	No	No
16511B	Yes	Yes	Yes	No	No	No	No	No
16515/16A	Yes	Yes	Yes	No	No	No	No	No
16517/18A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
16520/21A	Yes	Yes	Yes	No	No	No	No	No
16522A	No	Yes	Yes	Yes	Yes	Yes	Yes	No
16530/31A	Yes	Yes	Yes	No	No	No	No	No
16532A	Yes	Yes	Yes	No	No	No	No	No
16533A	No	No	Yes	Yes	Yes	Yes	Yes	No
16534A	No	No	Yes	Yes	Yes	Yes	Yes	No
16535A	No	Yes	Yes	Yes	No	No	No	No
16540/41A	Yes	Yes	Yes	No	No	No	No	No
16540/41D	Yes	Yes	Yes	No	No	No	No	No
16542A	Yes	Yes	Yes	No	No	No	No	No
16550A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
16554A	No	Yes	Yes	Yes	Yes	Yes	Yes	No
16555A/D	No	Yes	Yes	Yes	Yes	Yes	Yes	No
16556A/D	No	Yes	Yes	Yes	Yes	Yes	Yes	No
16557D	No	No	Yes	Yes	Yes	Yes	Yes	No
16710/11/12A	No	No	No	No	Yes	Yes	Yes	No
16715/16/17A	No	No	No	No	No	Yes	Yes	No
16718/19A	No	No	No	No	No	Yes	Yes	No
16720A	No	No	No	No	No	Yes	Yes	No
16740/41/42A	No	No	No	No	No	Yes †††	Yes †††	Yes
16750/51/52A	No	No	No	No	No	Yes †	Yes †	Yes
16750/51/52B	No	No	No	No	No	Yes †	Yes †	Yes
16753/54/55/56A	No	No	No	No	No	Yes ††††	Yes ††††	Yes
16760A	No	No	No	No	No	Yes††	Yes††	No
16910A/11A	No	No	No	No	No	No	No	Yes
16950A	No	No	No	No	No	No	No	Yes

† - Will work with software revision A.02.00.00
 †† - Will work with software revision A.02.20.00
 ††† - Will work with software revision A.02.50.00
 †††† - Will work with software revision A.02.70.00

For 16700 software updates please visit
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